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Photovoltaic based distribution static compensator for power quality improvement

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ABSTRACT

This paper deals with a model of photovoltaic (PV) array or battery operated DC/DC boost converter fed three-leg VSC (Voltage Source converter) with star delta transformer for power quality improvement. A synchronous reference frame theory is proposed for three-phase four-wire DSTATCOM (Distribution Static Compensator) which includes voltage source converter and a dc link capacitor. The proposed DSTATCOM provides reactive power compensation, source harmonic reduction and neutral current compensation at the point of common coupling (PCC). The PV array or battery operated boost converter is used to step up the voltage to match the DC link requirement of the three-leg VSC. The main advantage of this proposed approach is that, it will provide continuous compensation for the whole day. The star/delta transformer provides isolation to the VSC and path to the zero sequence fundamental as well as harmonics neutral current. To derive the reference current in order to generate the firing pulse to the VSC, the overall system is designed, developed and validated by using MATLAB–SIMULINK environment.

1. Introduction

In recent years many researchers have focused on renewable energy source based power quality improvement in the power distribution system because of widespread use of non-linear electronic loads [1,2]. There are different types of microsources which include photovoltaic cell, fuel cell and wind power [3–9]. However, fuel cell and photovoltaic cell are low voltage sources to provide enough DC voltage to obtain the AC voltage. The photovoltaic (PV) cell only has the facility to connect it in series to provide the necessary dc voltage. The power generated from the PV array needs power conditioning (i.e., DC/DC (or) DC/AC) before connecting it to the dc link [10–12]. Thus the DC/DC boost converter is mainly employed to increase the low PV voltage to high voltage level.

Three-phase four-wire distribution systems are facing severe power quality problems due to different non-linear loads and unplanned expansions of the distribution system. The power quality problems include harmonic currents, high reactive power burden, load unbalance, and excessive neutral current etc. [13]. The group of controllers used in the distribution system is known as Custom Power Devices (CPDs) and it provides solution to the power quality problems. The CPD consisting of Distribution Static Compensator (DSTATCOM), Dynamic Voltage Restorer (DVR) and Unified Power Quality Conditioner (UPQC) are used for compensating the power quality problems in the current, voltage and both current and voltage respectively.

Most of the commercial and industrial loads possess non-linear characteristics. Examples are computer loads, lighting ballasts, switched mode power supply, motor drive applications etc. These lead to harmonics in the supply current as well as excessive neutral current. The zero sequence neutral current gets a path through the neutral conductor. The neutral current mainly consists of third harmonics current [14]. The unbalanced single-phase loads result in high neutral current. Different mitigation solutions for these power quality problems are SVC, STATCOM etc. The SVC used at transmission level with limited bandwidth and higher values of passive elements increase its size and losses, slows the response and make them inapt. Similarly, STATCOM can also provide reactive power compensation and voltage support only at the transmission level. But the DSTATCOM has the capacity to overcome the above drawbacks with faster response which can be employed at the distribution side [15]. The different topologies of DSTATCOM for three-phase four-wire system for the mitigation of reactive power compensation, harmonic reduction in the source current, neutral current compensation and load balancing, are four-leg Voltage Source Converter (VSC), three single phase VSC, three-leg VSC with split capacitor [14] and three-leg VSC with neutral terminal positive or negative of dc bus [16]. Among the different control techniques applied to the three-phase four-wire compensators, the synchronous reference frame theory technique is suitable for the control of DSTATCOM [17].

The main aim of this paper is to maintain the dc link voltage of the three-leg VSC to provide continuous compensation. The

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purpose of photovoltaic (PV) array is to drive the boost converter to step-up the voltage and maintain the dc link voltage. When continuous compensation is required, the PV array is connected to the boost converter in the day time and during the night time battery acts as a dc source for the boost converter. When excess power is available or compensation is not required the PV array charges the battery. The boost converter presented in this paper utilizes a pulse width modulation technique. By using this technique the boost converter draws constant power from the source. This paper does not discuss the maximum power point algorithm. The three-leg VSC utilizing fast switching insulated gate bipolar transistor (IGBT) with a dc bus capacitor is mainly employed for the required compensation. The star/delta transformer is used to mitigate the neutral current by providing a circulating path in the delta connected secondary winding [18] and the DSTATCOM is connected in shunt with the load with an isolation transformer [19].

2. Design of DSTATCOM and star/delta transformer

The power circuit of boost converter fed three-leg VSC with star/delta transformer is connected to point of common coupling (PCC) with nonlinear load is shown in Fig. 1. The VSC consists of insulated-gate bipolar transistors (IGBTs), inductors and dc capacitors. The value of the dc bus voltage of VSC based DSTATCOM mainly depends on the instantaneous energy available to the DSTATCOM [20]. The dc bus voltage is calculated as follows:

$$V_{\mathrm{dc}} = \frac{2\sqrt{2}V_{\mathrm{LL}}}{\sqrt{3}m} \tag{1}$$

where m is the modulation index considered as 1 and V_{LL} the line to line voltage. Thus V_{dc} is obtained as 677.69 V for V_{LL} of 415 V and it is selected as 680 V.

The value of dc capacitor (C_{dc}) of VSC based DSTATCOM depends on the instantaneous energy available to the DSTATCOM during transients [20]. The dc capacitor is calculated as follows:

$$\frac{1}{2}C_{\mathrm{dc}}\left[\left(V_{\mathrm{dc}}^2\right) - \left(V_{\mathrm{dc}}^2\right)\right] = 3V(aI)t \tag{2}$$

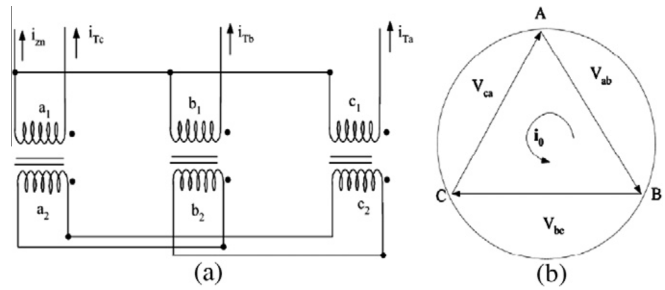

Fig. 2. (a) Star/delta transformer windings. (b) Phasor diagram.

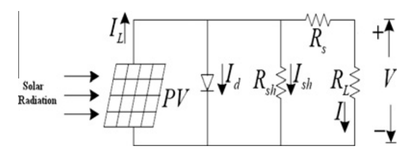

Fig. 3. Equivalent electrical circuit of PV cell.

where V_{dc} is the reference dc voltage and V_{dc1} the minimum voltage level of dc bus, a the overloading factor, V the phase voltage, I the phase current, and t the time by which the dc bus voltage is to be recovered. Considering $V_{\mathrm{dc}} = 680$ V, $V_{\mathrm{dc1}} = 670$ V, $V = 415/\sqrt{3} = 239.6$ V, $I = 58.13$ A, $t = 350$ μs and $a = 1.2$, the calculated value of C_{dc} is 2600 μF. So C_{dc} the chosen to be 3000 μF.

Fig. 2a and b shows the connection and the voltage phasor diagram of star/delta transformer. The current rating of the transformer is based on circulating current i_o, in case of any zero sequence current and the compensation current provided by the VSC. The primary winding voltage of 240 V is selected for star/delta transformer when the line to line voltage is 415 V. The secondary line voltage is chosen for the same current to flow in the windings and the voltage ratio of the transformer is 1:1. A ripple filter is used for reducing the ripple voltage due to switching current of the VSC at the point of common coupling (PCC).

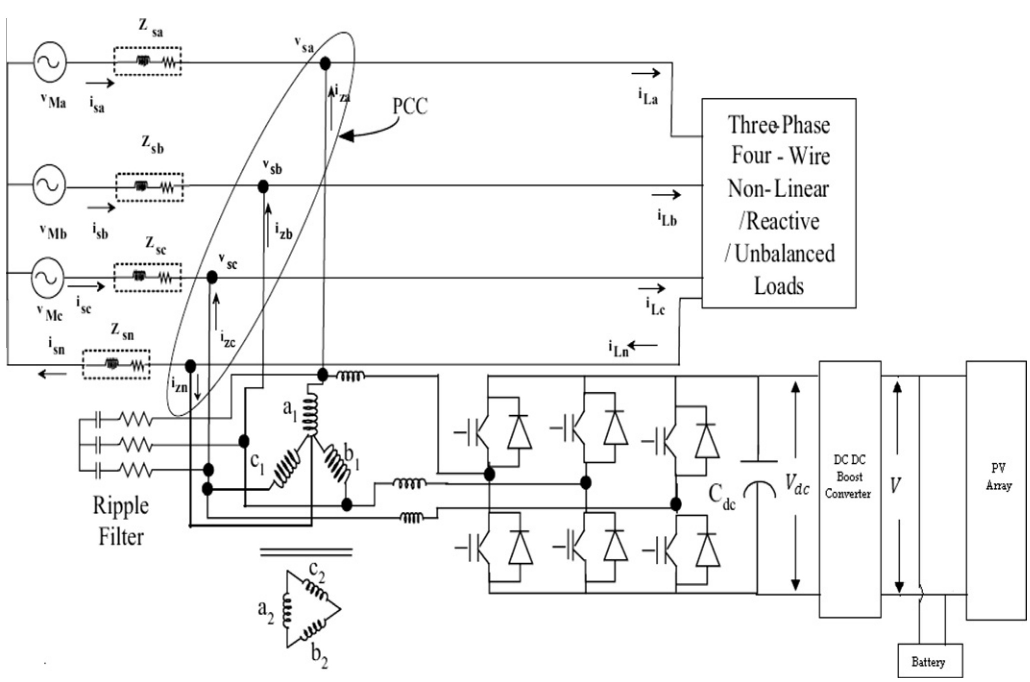

Fig. 1. Schematics of proposed renewable based three-leg VSC with star/delta transformer.

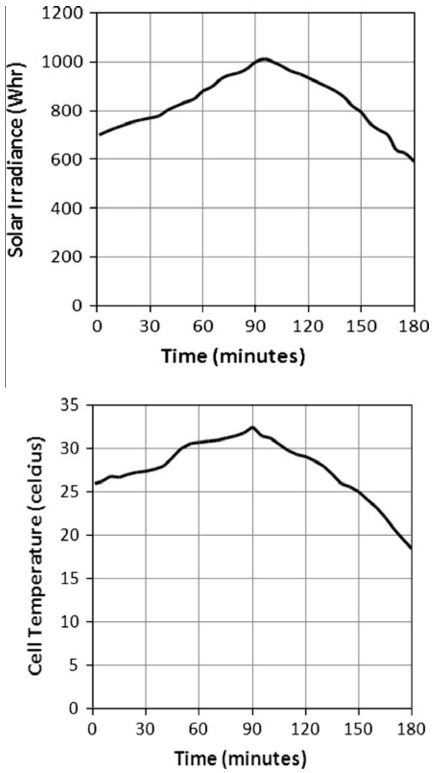

Fig. 4. Solar irradiance and cell temperature.

3. Modeling of photovoltaic array

The PV array is a group of several modules connected in series to obtain a required current and voltage. The theory of photovoltaic cell is the photovoltaic effect of the semiconductor material. The equivalent electrical circuit of the PV cell is shown in Fig. 3. Due to the sudden changes in weather conditions, the external influences like solar irradiation level and the cell operating temperature will change with time as shown in Fig. 4. In India, next to the states Rajasthan and Gujarat, Tamilnadu receives about 5.35 Kwh/sq m/day and this is the third largest amount of solar radiation in India. The solar radiation level in Tamilnadu is shown in Fig. 5. The solar arrays are built up with combined series/parallel combination of solar cells inorder to maintain the *I*–*V* characteristics.

Table 1
Parameters of Sanyo HIT-240HDE4 solar panel.

Parameters	Symbol	Typical value
Rated maximum power	P_{mp}	240 W
Open circuit voltage	V_{oc}	43.6
Short circuit current	I_{sc}	7.37
Rated voltage	V	35.5
Rated current	I	6.77
Short circuit temperature coefficient	K_I	2.21 mA/°C
Open circuit temperature coefficient	K_V	1.0.109 V/°C
Number of cells	–	6 × 10

To model the PV module in MATLAB–SIMULINK, the parameters are obtained from SANYO-240HDE4 datasheet at solar irradiance of 1000 W/m^2 and temperature of 25 °C are shown in Table 1. The PV module having 60 Heterojunction with Intrinsic Thin Layer (HIT) silicon cell are connected to obtain a desired voltage of 36 V. This solar cell has an advantage to generate more energy than conventional crystal solar cells [21]. The *I*–*V* characteristics of PV module at variable solar irradiance with constant temperature of 25 °C and variable temperature with constant solar irradiance of 1000 W/m^2 are shown in Fig. 6. The PV model is developed using basic equations of photovoltaic cells including the effects of temperature and solar irradiation [22–24]. The diode current and load current equations are given by the following relations,

$$I_{\rm d} = I_{\rm sat}\left(e^{\frac{QV_{oc}}{AkT}} - 1\right) \quad (3)$$

$$I = I_{\rm L} - I_{\rm sat}\left(e^{\frac{QV_{oc}}{AkT}} - 1\right) - \frac{V_{oc}}{R_{sh}} \quad (4)$$

The maximum photovoltaic voltage is obtained under open circuit condition (i.e), when $I = 0$ and is given by

$$V_{oc} = \frac{AkT}{Q}\log_n\left(\frac{I_{\rm L}}{I_{\rm sat}} + 1\right) \quad (5)$$

where I_{sat} is the saturation current of the diode (10^{-4} A), Q the electron charge (1.602×10^{-19} Coulomb), A the curve fitting constant, K the Boltzmann constant (1.38×10^{-23} J/K), T the operating temperature in absolute scale (40 °C), $I_{\rm L}$ the photovoltaic current in Ampere, V_{oc} the open circuit voltage and R_{sh} the shunt resistance (200–300 Ω).

The operation of the proposed DSTATCOM has been divided into three modes. The modes are (i) day time excess power mode, (ii) day time mode, (iii) night time mode.

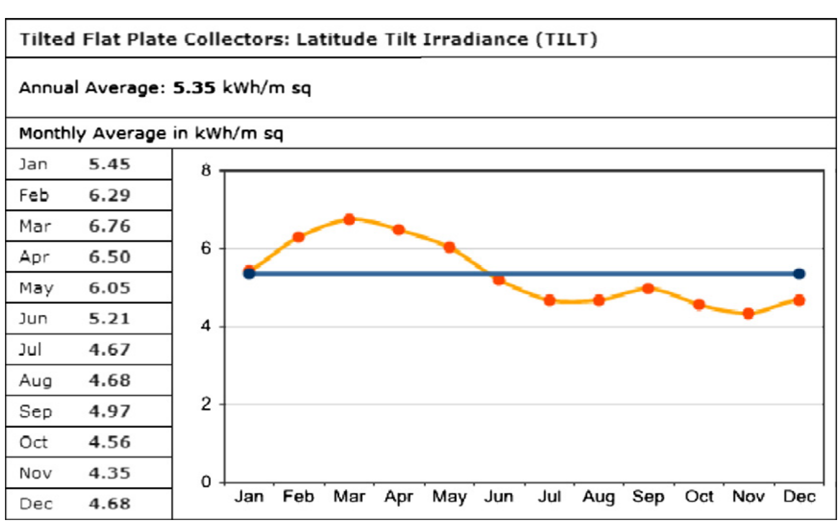

Fig. 5. Solar radiation level in Tamilnadu (January 2011–December 2011).

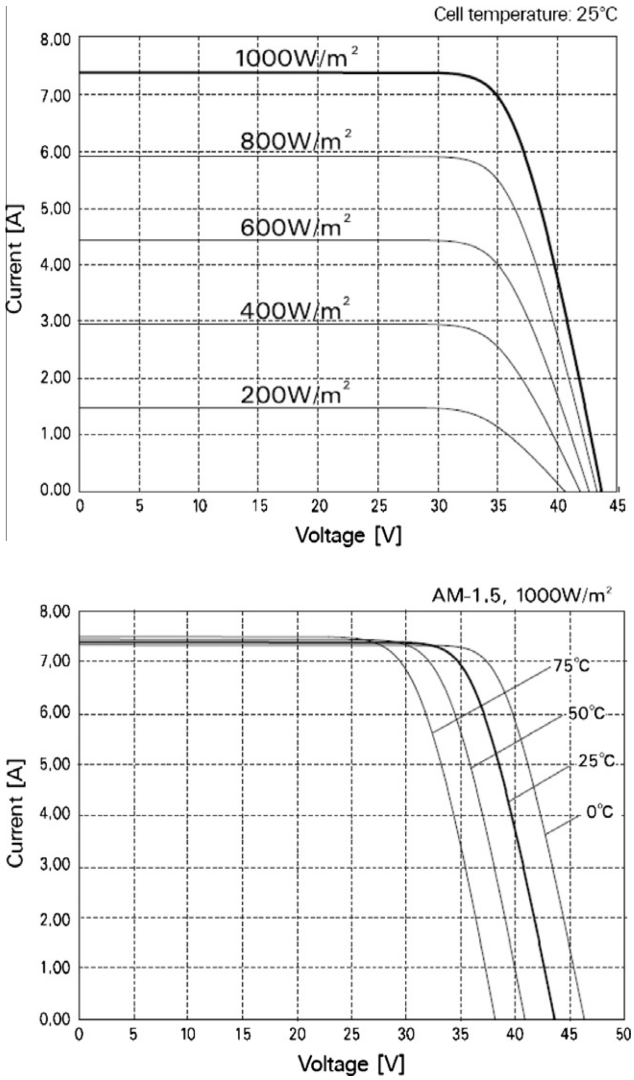

Fig. 6. *I–V* characteristics of SANYO-240HDE4 PV Module.

i. *Day time excess power mode*. In this mode, the output voltage of the PV array drives the boost converter based DSTATCOM for compensating the source as well as charges the 36 V battery.
ii. *Day time mode*. When continuous compensation is required, if the PV output voltage is equal to the requirement of the boost converter input, the PV array can directly connect to the boost converter so as to step-up the voltage and match the dc link voltage of the three-leg VSC. In this mode, the battery is not charged.
iii. *Night time mode*. In this mode, PV output is absent and only the battery supplies the boost converter for providing compensation at the night time.

4. Control of DC link voltage with boost converter

The boost converter is used to step up the input voltage to obtain a desired output voltage. The PV array or battery operated boost converter is shown in Fig. 7. The circuit operation is divided into two modes. In mode 1, when the switch is in on condition the input current supplies energy to the inductor for a period T_{on}. Similarly in mode 2, when the switch is off, the inductor voltage adds to the source voltage and current is forced to flow through diode *D* and the load for a period T_{off}. The PV or battery voltage of 36 V is

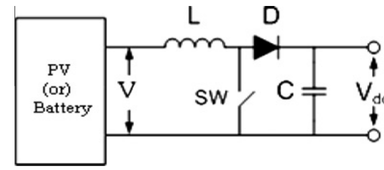

Fig. 7. Topology of PV or battery operated boost converter.

fed to the boost converter and the output voltage of the boost converter of 676 V is obtained to maintain the dc link voltage of the three-leg voltage source converter. In order to step-up the voltage, a switching frequency of 25 kHz is considered and the inductor value of 0.0191 mH is calculated [25,26]. The capacitor *C* of 3000 μF is chosen as per Eq. (2). The output voltage V_{out} is greater than the input Voltage V_{in} and the output equation is shown in the following equation.

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \quad \text{where } V_{out} = V_{dc},\ V_{in} = V \text{ and } D = \frac{T_{on}}{T_{on}+T_{off}} \tag{6}$$

where *V is the PV or battery voltage, D the duty cycle,* T_{on} the on time, and T_{off} the off time.

5. Control of DSTATCOM

There are many control algorithms available for the generation of reference source currents for the control of proposed DSTATCOM in the literature viz. synchronous reference frame theory, instantaneous reactive power theory (p–q theory), power balance theory etc. [17,27,28]. The synchronous reference frame theory is found suitable for the control of VSC. A block diagram of the controlling algorithm is shown in Fig. 8.

The feedback signals are sensed from the load currents, PCC voltages and dc bus voltages of DSTATCOM. The load currents from the a–b–c frame are first converted to α–β–0 frame and then to d–q–0 frame using the following equation,

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{2} \\ \cos\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta-\frac{2\pi}{3}\right) & \frac{1}{2} \\ \cos\left(\theta+\frac{2\pi}{3}\right) & \sin\left(\theta-\frac{2\pi}{3}\right) & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \end{bmatrix} \tag{7}$$

A three phase PLL (phase locked loop) is used to synchronize these signals with the PCC voltage. The dc component of i_d and i_q are obtained by passing a d–q–0 current component through the low pass filter. The input of first PI (Proportional Integral) controller is the error between the reference dc bus voltage (V_{dc}^*) and the sensed dc bus voltage (V_{dc}) of DSTATCOM. The output of PI controller is the loss component of the current (i_{loss}).

$$i_{loss(n)} = i_{loss(n-1)} + k_{pd}(V_{de(n)} - V_{de(n-1)}) + K_{id}\, v_{de(n)} \tag{8}$$

where $V_{de(n)}$ is the error between reference and sensed dc voltage at the *n*th sampling instant. K_{pd} and K_{id} are the proportional and integral gains of the dc bus voltage PI controller. Therefore the reference source current is,

$$i_d^* = i_{ddc} + i_{loss} \tag{9}$$

Similarly, the amplitude of actual PCC voltage and its reference value are fed to another PI controller for regulating the PCC voltage. The output of the PI controller is added to the dc component of i_q because this is a quadrature component of current for regulating the ac voltage.

$$i_{qr(n)} = i_{qr(n-1)} + K_{pq}(V_{te(n)} - V_{te(n-1)}) + K_{iq}\, v_{te(n)} \tag{10}$$

where $V_{de(n)}$ is the error between reference (V_s^*) and sensed supply voltage ($V_{s(n)}$) amplitude at the *n*th sampling instant. The

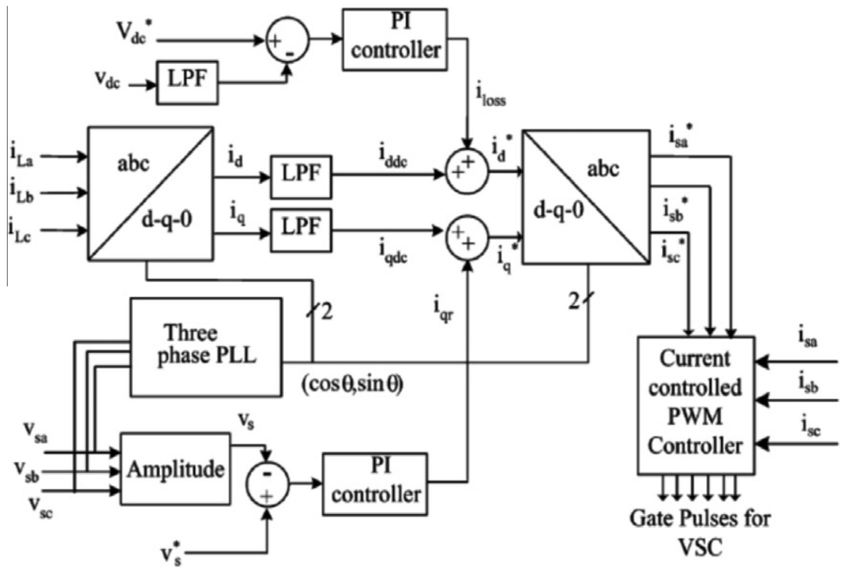

Fig. 8. Control algorithm of three leg VSC.

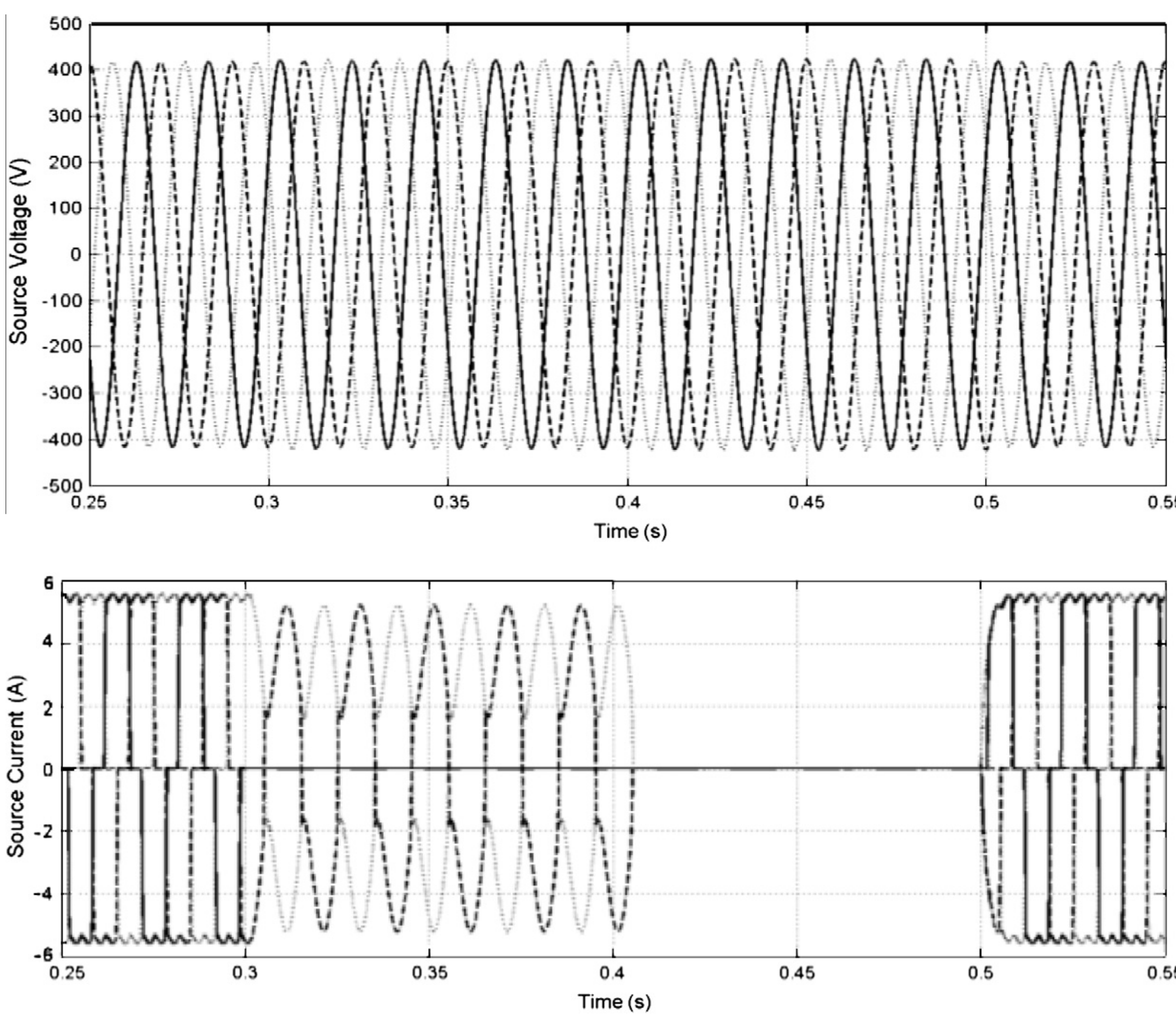

Fig. 9a. Performance of source voltage and source current without compensation.

proportional and integral gains of the PCC voltage PI controller are K_{pq} and K_{iq}. The reference supply quadrature axis current is,

$$i_q^* = i_{qdc} + i_{qr} \tag{11}$$

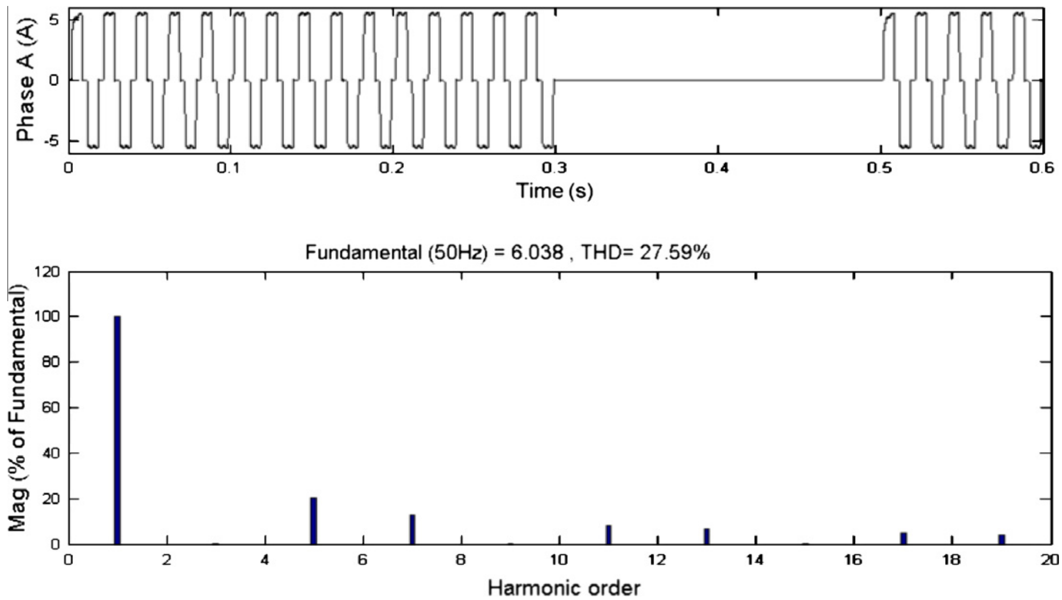

Fig. 9b. Performance of phase A load current with its spectrum without compensation.

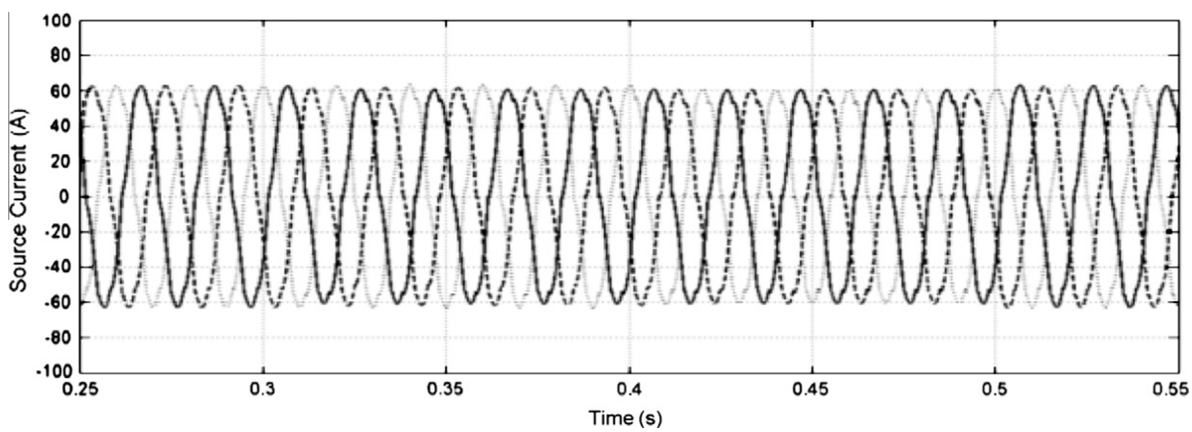

Fig. 9c. Source current after compensation.

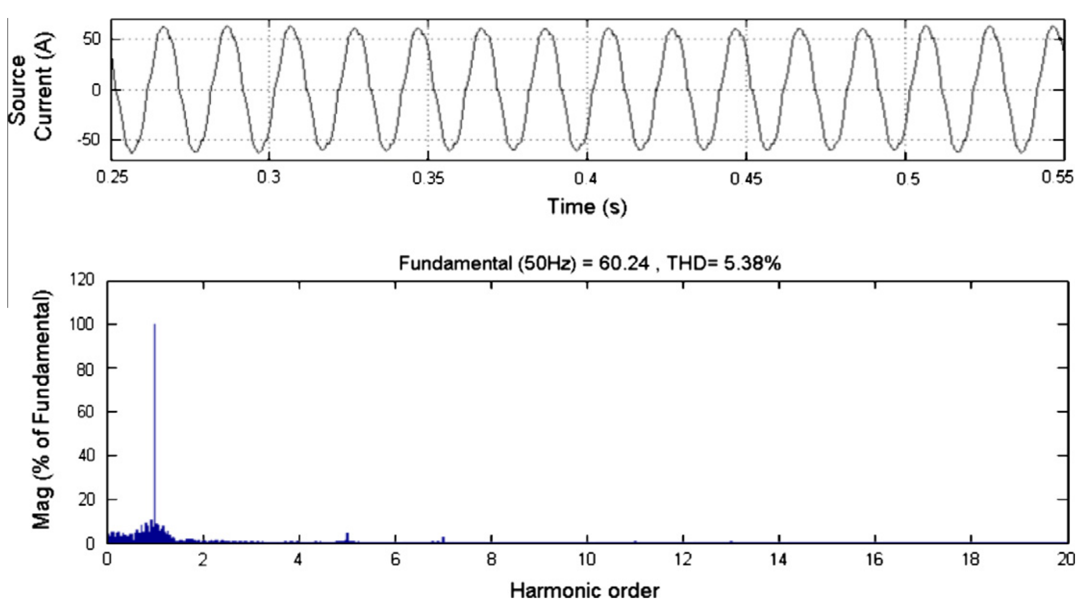

Fig. 9d. Source current for phase A with its spectrum after compensation.

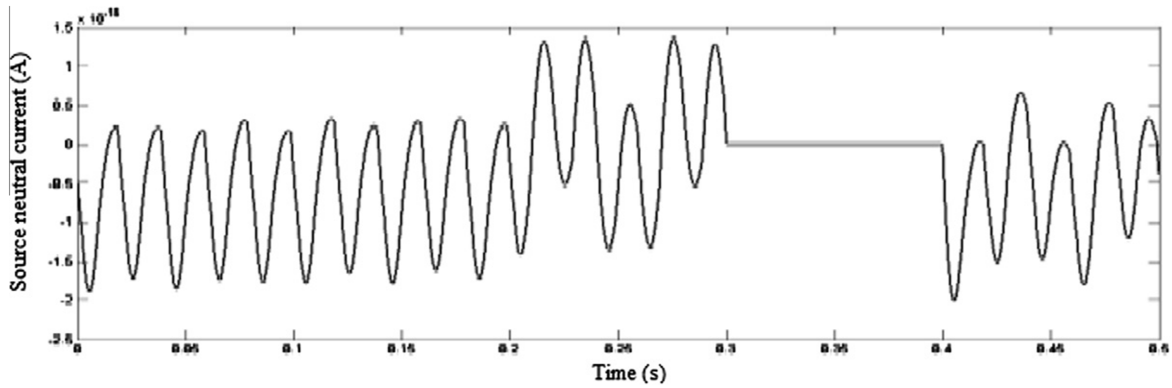

Fig. 9e. Source neutral current after compensation.

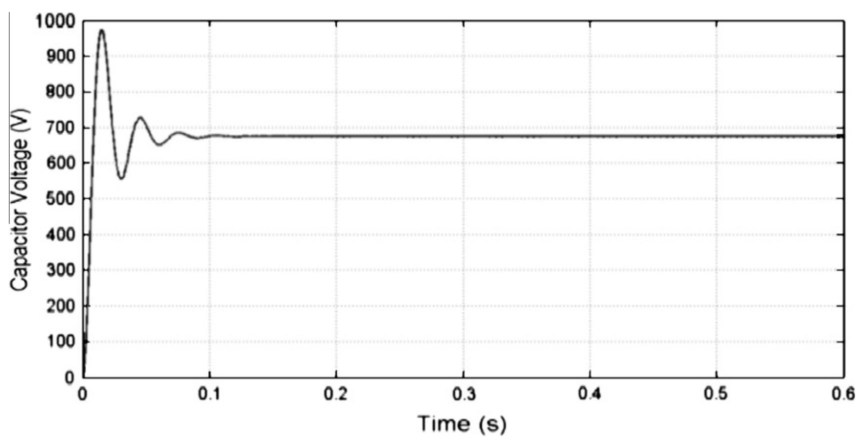

Fig. 9f. Capacitor voltage after compensation.

Table 2
Source current total harmonic distortion (THD) for boost converter fed three-leg VSC.

THD in all three phases	Three-leg VSC based DSTATCOM with diode bridge rectifier	
	Without compensation	With compensation
THD of phase A	27.59	5.38
THD of phase B	27.60	5.65
THD of phase C	27.60	5.82

By using reverse Park's transformation, the resultant d–q–0 currents are again converted back to reference source currents. The reference currents in all the three phases $(i^*_{sa}, i^*_{sb}, i^*_{sc})$ are used for generating the gate pulses for three-leg VSC based DSTACOM. A PWM current controller is used for generating the gating signals for the IGBT's in VSC by using the reference and sensed source currents.

6. Results and discussion

The boost converter fed three-leg VSC with the star/delta transformer based DSTATCOM in a three-phase four-wire system which is modeled and simulated by using the MATLAB with its SIMULINK environment and PSB toolboxes. The electrical power system under nonlinear load condition for source voltage and source current without compensation is shown in Fig. 9a. The source current for phase A and its harmonic spectrum without compensation is shown in Fig. 9b. At 0.3 s, the load is changed to two phase load and also the load currents are made zero between 0.4 s and 0.5 s. These loads are applied again at 0.5 s respectively. The source current is still sinusoidal even when the load in a phase is zero as shown in Fig. 9c. It is observed from the waveform that the harmonic current is compensated and source current is made sinusoidal. The source current for phase A and its harmonic spectrum after compensation is shown in Fig. 9d and the source neutral current is shown in Fig. 9e. The capacitor voltage waveform after compensation is shown in Fig. 9f. The electrical power system data used for simulation is given in Appendix A. The parameter of the photovoltaic system is given in Table 1. The total harmonic distortion for the proposed DSTATCOM is given in Table 2.

7. Conclusion

The performance of three-phase four-wire DSTATCOM consisting of PV or battery operated boost converter fed three-leg VSC with a star/delta transformer is extensively simulated in MATLAB/SIMULINK software. A synchronous reference frame method has been presented in the paper for reactive power compensation, source harmonic reduction, and neutral current compensation. The boost converter is used to step up the voltage so as to match the dc link voltage of the three-leg VSC and the star/delta transformer has compensated the neutral current. It is observed that the THD (Total Harmonic Distortion) of the source current for phase A is reduced from 27.59 to 5.38.

Appendix A

3-phase AC line voltage: 415 V, 50 Hz.
Line impedance: R_s = 0.01 Ω, L_s = 2 mH per phase.

Non-linear load: Three phase bridge rectifier with RL.
Ripple filter: $R_f = 5\ \Omega$, $C_f = 5\ \mu F$.
AC inductor: 3.3 mH.
DC bus capacitor of DSTATCOM, C_{dc}: 3000 μF.
DC bus voltage of DSTATCOM: 680 V.
DC voltage PI controller: $K_{pd} = 0.2$, $K_{id} = 1$.
PCC voltage PI controller: $K_{pq} = 0.01$, $K_{iq} = 2$.

References

[1] Singh Mukhtiar, Khadkikar Vinod, Chandra Ambrish, Varma Rajiv K. Grid Interconnection of renewable energy sources at the distribution level with power quality improvement features. IEEE Trans Power Deliv 2011;26(1):307–15.
[2] Pinto JP, Pregitzer R, Monteiro LFC, Afonso JL. 3-Phase 4-wire shunt active filter with renewable energy interface. Presented at the conference IEEE renewable energy & power quality, Seville, Spain; 2007.
[3] Jan T, Bialasiewicz. Renewable energy systems with photovoltaic power generators: operation and modeling. IEEE Trans Ind Electron 2008;55(7):2752–8.
[4] Lo Y, Lee T, Wu K. Grid-connected photovoltaic system with power factor correction. IEEE Trans Ind Electron 2008;55(5):2224–7.
[5] Dursun Erkan, Kilic Osman. Comparative evaluation of different power management strategies of a stand-alone PV/Wind/PEMFC hybrid power system. Int J Electr Power Energy Syst 2012;34(1):81–9.
[6] Wang Yong, Cai Xu. DC link voltage optimized control for efficient residential fuel cell converter. Int J Electr Power Energy Syst 2010;32(9):1031–6.
[7] Changchien SK, Liang TJ, Chen JF, Yang S. Novel high step-up DC–DC converter for fuel cell energy conversion system. IEEE Trans Ind Electron 2010;57(6):2007–17.
[8] Suvire Gaston O, Mercado Pedro E. Improvement of power quality in wind energy applications using a DSTATCOM coupled with a flywheel energy storage system. Power Electron Conf 2009:58–64.
[9] Oshiro Masato, Funabashi Toshihisa, Kim Chul-Hwan. Optimal voltage control in distribution systems using PV generators. Int J Electr Power Energy Syst 2011;33(3):485–92.
[10] Blaabjerg F, Teodorescu R, Liserre M, Timbus AV. Overview of control and grid synchronization for distributed power generation systems. IEEE Trans Ind Electron 2006;53(5):1398–409.
[11] Carrasco JM, Franquelo LG, Bialasiewicz JT, Galván E, Guisado RCP, Prats MAM, et al. Power Electronic systems for the grid integration of renewable energy sources: a survey. IEEE Trans Ind Electron 2006;53(4):1002–16.
[12] Renders B, De Gusseme K, Ryckaert WR, Stockman K, Vandevelde L, Bollen MHJ. Distributed generation for mitigating voltage dips in low-voltage distribution grids. IEEE Trans Power Deliv Jul. 2008;23(3):1581–8.
[13] Mei Xue, Weilin Wu, Chen Xiaodong. Analysis of power quality variations. IEEE Conf 2003;1:41–4.
[14] Akagi H, Watanabe EH, Aredes M. Instantaneous power theory and applications to power conditioning. USA: John Wiley & Sons; 2007.
[15] Masand Deepika, Jain Shailendra, Agnihotri Gayatri. Control Strategies for Distribution Static Compensator for Power Quality Improvement. IETE Journal of Research 2008;54(6):421–8.
[16] Jou HL, Wu KD, Li CH, Huang MS. Noval power converter topology for three phase four wire hybrid power filter. IET Power Electron 2008;1(1):164–73.
[17] Milanes Maria Isabel, Cadaval Enrique Romero, Gonzalez Fermin Barrero. Comparison of control strategies for shunt active power filters in three-phase four-wire systems. IEEE Trans Power Electr 2007;22(1):229–36.
[18] Enjeti P, Shireen W, Packebush P, Pitel I. Analysis and design of a new active power filter to cancel neutral current harmonics in three-phase four-wire electric distribution systems. IEEE Trans Ind Appl 1994;30(6):1565–72.
[19] Molina MG, Mercado PE. Control, design and simulation of DSTATCOM with energy storage for power quality improvements. Proc of TDC 2006;06:1–7.
[20] Singh BN, Rastgoufard P, Singh B, Chandra A, Haddad K. Al, design, simulation and implementation of three pole/four pole topologies for active filters. IEE Electric Power Appl 2004;151(4):467–76.
[21] <http://www.posharp.com/hit-240hde4-solar-panel-from-sanyoelectric_p2075938320d.aspx>.
[22] Altas H, Sharaf AM. A photovoltaic array simulation model for MATLAB Simulink GUI environment. In: Proc ICCEP '07; 2007. p. 341–5.
[23] Park M, Yu In-K. A novel real-time simulation technique of photovoltaic generation systems using RTDS. IEEE Trans Energy Convers 2004;19(1):164–9.
[24] PV module Simulink models. <http://ecewww.colorado.edu/~ecen2060/matlab.html>.
[25] Wei Jiang, Yu-fei Zhou, Jun-ning Chen. Modeling and simulation of boost converter in CCM and DCM. In: IEEE conference; 2009. p. 288–91.
[26] Mazouz N, Midoun A. Control of a DC/DC converter by fuzzy controller for a solar pumping system. Int J Electr Power Energy Syst 2011;33(10):1623–30.
[27] Singh Bhim, Jayaprakash P, Kothari DP. New control approach for capacitor supported DSTATCOM in three-phase four wire distribution system under non-ideal supply voltage conditions based on synchronous reference frame theory. Int J Electr Power Energy Syst 2011;33(5):1109–17.
[28] Benhabib MC, Saadate S. New control approach for four-wire active power filter based on the use of synchronous reference frame. Electr Power Syst Res 2005;73(3):353–62.