A Novel Transformer-less Adaptable Voltage Quadrupler DC Converter with Low Switch Voltage Stress

Ching-Tsai Pan, *Member, IEEE*, Chen-Feng Chuang, and Chia-Chi Chu, *Member, IEEE*

***Abstract*—In this paper, a novel transformer-less adjustable voltage quadrupler dc–dc converter with high-voltage transfer gain and reduced semiconductor voltage stress is proposed. The proposed topology utilizes input-parallel output-series configuration for providing a much higher voltage gain without adopting an extreme large duty cycle. The proposed converter cannot only achieve high step-up voltage gain with reduced component count but also reduce the voltage stress of both active switches and diodes. This will allow one to choose lower voltage rating MOSFETs and diodes to reduce both switching and conduction losses. In addition, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the two interleaved phases for voltage boosting mode without adding extra circuitry or complex control methods. The operation principle and steady analysis as well as a comparison with other recent existing high step-up topologies are presented. Finally, some simulation and experimental results are also presented to demonstrate the effectiveness of the proposed converter.**

***Index Terms*—Automatic uniform current sharing, high step-up converter, low voltage stress, transformer-less, voltage quadrupler.**

I. Introduction

With global energy shortage and strong environmental movements, renewable or clean energy sources such as solar cells and fuel cells are increasingly valued worldwide. However, due to the inherent low voltage characteristic of these sources, a high step-up dc converter is essential as a prestage of the corresponding power conditioner. The conventional boost and buck–boost converters, due to the degradation in the overall efficiency as the duty ratio approaches unity [1], obviously cannot fulfill the application need. Besides, the extreme duty ratio not only induces very large voltage spikes and increases conduction losses but also induces severe diode reverse-recovery problem [2], [3]. Many topologies have been presented to provide a high step-up voltage gain without an extremely high duty ratio as can be seen from the review paper [4]. A dc–dc flyback converter is a very simple isolated structure with a high step-up voltage gain, but the active switch of this converter will suffer a high voltage stress due to the leakage inductance of the transformer. For recycling the energy of the leakage inductance and minimizing the voltage stress of the active switch, some energy-regeneration techniques have been proposed to clamp the voltage stress on the active switch and to recycle the leakage-inductance energy [5]–[7]. Some existing isolated voltage-type converters, such as the phase-shifted full-bridge converters, can achieve a high step-up gain by increasing the turns ratio of the transformer. Unfortunately, the higher input current ripple will reduce the maximum output power and shorten the usage life of input electrolytic capacitor. To reduce the effects, more input electrolytic capacitors are required to suppress the large input current ripple. Furthermore, the output diode voltage stress is much higher than the output voltage, which will degrade the circuit efficiency in the high-output-voltage applications. Other isolated current-type converters, such as the active-clamp dual-boost converters and the active-clamp full-bridge boost converters [8], [9], can realize high efficiency and high step-up conversion. However, the start-up operation of these converters must be considered separately. Moreover, the cost is increased because many extra power components and isolated sensors or feedback controllers are required. In order to reduce system cost and to improve system efficiency, a nonisolated dc/dc converter is, in fact, a more suitable solution [10], [11].

The switched capacitor-based converters proposed in [12]–[15] provide solutions to improve the conversion efficiency and achieve large voltage conversion ratio. Unfortunately, the conventional switched capacitor technique makes the switch suffer high transient current and large conduction losses. Furthermore, many switched capacitor cells are required to obtain extremely high step-up conversion, which increases the circuit complexity [27]. However, recently a study on energy efficiency of switched-capacitor converters was presented in [33]; the authors presented some design rules useful for developing high-efficiency switched-capacitor converters, based on their analysis. In [34], several modular converter topologies were presented based on a switched-capacitor cell concept in which a soft-switched scheme was used to reduce the switching loss and electromagnetic interference [35], [36].

The coupled inductor-based converters are another solution to implement high step-up gain because the turns ratio of the coupled inductor can be employed as another control freedom to extend the voltage gain [16]–[18], [29], [31]. However, the

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input current ripple is relatively larger by employing single-stage single-phase-coupled inductor-based converters, which may shorten the usage life of the input electrolytic capacitor [27]. As such, a family of interleaved high step-up boost converters with winding-cross-coupled inductors is proposed in [19]–[21], [30]. The active clamp or passive lossless clamp circuits are adopted to achieve soft-switching operation. Alternatively, some interleaved high step-up converters with simplified coupled inductors are introduced to derive more compact circuit structure [22], [23], [32].

The interleaved voltage doubler [24] has been proposed for universal line power factor correction front end with automatic current sharing capability and lower active switch stress to increase the low-line efficiency. However, the voltage gain is not high enough and the diode voltage stress remains very high [28]. To achieve higher voltage conversion ratio and further reduce voltage stress on the switch and diode, the high step-up ratio converter [25] and the ultrahigh step-up converter [26] have been proposed. These converters can provide large step-up voltage conversion ratios. Unfortunately, the voltage stress of diodes in those converters remains rather high.

In this paper, a novel transformer-less adjustable voltage quadrupler topology is proposed. It integrates two-phase interleaved boost converter to realize a high voltage gain and maintain the advantage of an automatic current sharing capability simultaneously. Furthermore, the voltage stress of active switches and diodes in the proposed converter can be greatly reduced to enhance overall conversion efficiency.

The remaining contents of this paper may be outlined as follows. First, the novel circuit topology and operation principle are given in Section II. Then, the corresponding steady-state analysis is made in Section III to provide some basic converter characteristics. A prototype is then constructed and some simulation and experimental results are then presented in Section IV for demonstrating the merits and validity of the proposed converter. Finally, some conclusions are offered in the last section.

II. Operating Principle of the Proposed Converter

For convenient reference, the two-phase interleaved boost converter with parallel-input series-output connection is first shown in Fig. 1(a). The proposed converter topology is basically derived from a two-phase interleaved boost converter and is shown in Fig. 1(b). Comparing Fig. 1(a) with Fig. 1(b), one can see that two more capacitors and two more diodes are added so that during the energy transfer period partial inductor stored energy is stored in one capacitor and partial inductor stored energy together with the other capacitor store energy is transferred to the output to achieve much higher voltage gain. However, the proposed voltage gain is twice that of the interleaved two-phase boost converter. Also, the voltage stress of both active switches and diodes are much lower than the latter. Furthermore, as will be obvious latter, the proposed converter possesses automatic uniform current sharing capability without adding extra circuitry or complex control methods. The detailed operating principle can be illustrated as follows.

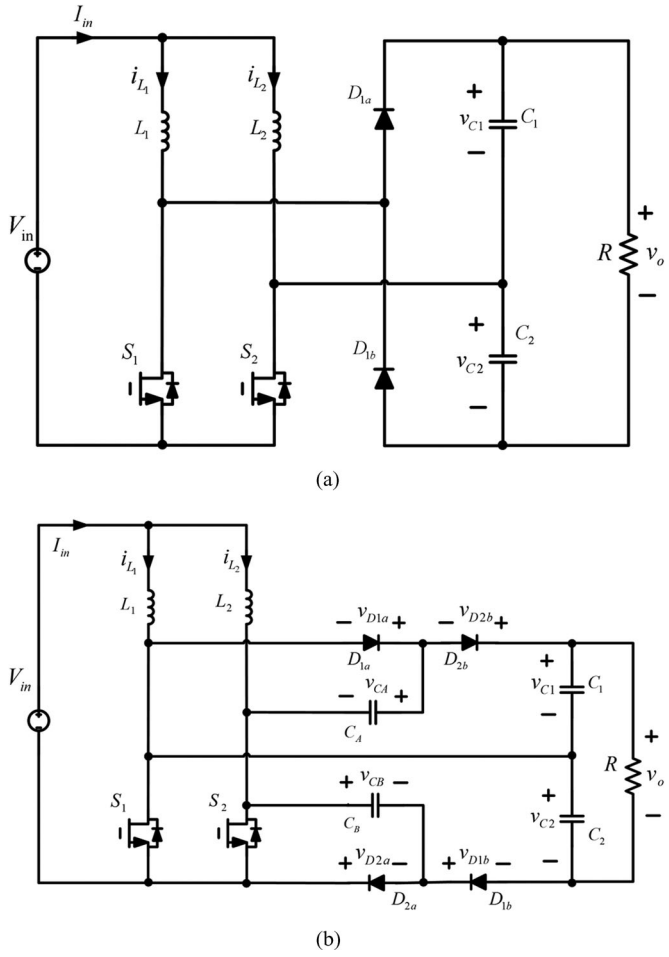

Fig. 1. Configurations of (a) two-phase interleaved boost converter (b) the proposed converter.

The proposed converter topology, like any existing high step-up dc converter, possesses the drawback of existence of pulsating output period. Furthermore, as the main objective is to obtain high voltage gain and such characteristic can only be achieved when the duty cycle is greater than 0.5 and in continuous conduction mode (CCM); hence, the steady-state analysis is made only for this case. However, with duty cycle lower than 0.5 or in DCM, as there is no enough energy transfer from the inductors to the blocking capacitors, output capacitors, and load side, and consequently it is not possible to get the high voltage gain as that for duty ratio greater than 0.5. In addition, only with duty cycle larger than 0.5, due to the charge balance of the blocking capacitor, the converter can feature the automatic current sharing characteristic that can obviate any extra current-sharing control circuit. On the other hand, when duty cycle is smaller than 0.5, the converter does not possess the automatic current sharing capability any more, and the current-sharing control between each phases should be taken into account in this condition.

In order to simplify the circuit analysis of the proposed converter, some assumptions are made as follows.

1) All components are ideal components.
2) The capacitors are sufficiently large, such that the voltages across them can be considered as constant approximately.

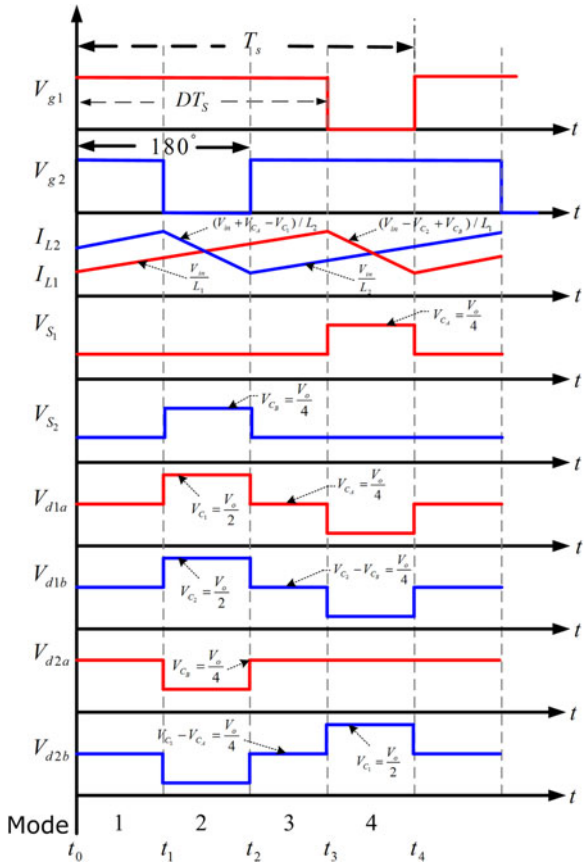

Fig. 2. Key operating waveforms of the proposed converter at CCM.

3) The system is under steady state and is operating in CCM and with duty ratio being greater than 0.5 for high step-up voltage purpose.

Basically, the operating principle of the proposed converter can be classified into four operation modes. The interleaved gating signals with a 180 ° phase shift as well as some key operating waveforms are shown in Fig. 2.

Mode 1 ($t_0 \le t < t_1$): For mode 1, switches S_1 and S_2 are turned ON, $D_{1a}, D_{1b}, D_{2a}, D_{2b}$ are all OFF. The corresponding equivalent circuit is shown in Fig. 3(a). From Fig. 3(a), it is seen that both i_{L1} and i_{L2} are increasing to store energy in L_1 and L_2, respectively. The voltages across diodes D_{1a} and D_{2a} are clamped to capacitor voltage V_{CA} and V_{CB}, respectively, and the voltages across the diodes D_{1b} and D_{2b} are clamped to V_{C2} minus V_{CB} and V_{C1} minus V_{CA}, respectively. Also, the load power is supplied from capacitors C_1 and C_2. The corresponding state equations are given as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{in} \tag{1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} \tag{2}$$

$$C_A \frac{dv_{C_A}}{dt} = 0 \tag{3}$$

$$C_B \frac{dv_{C_B}}{dt} = 0 \tag{4}$$

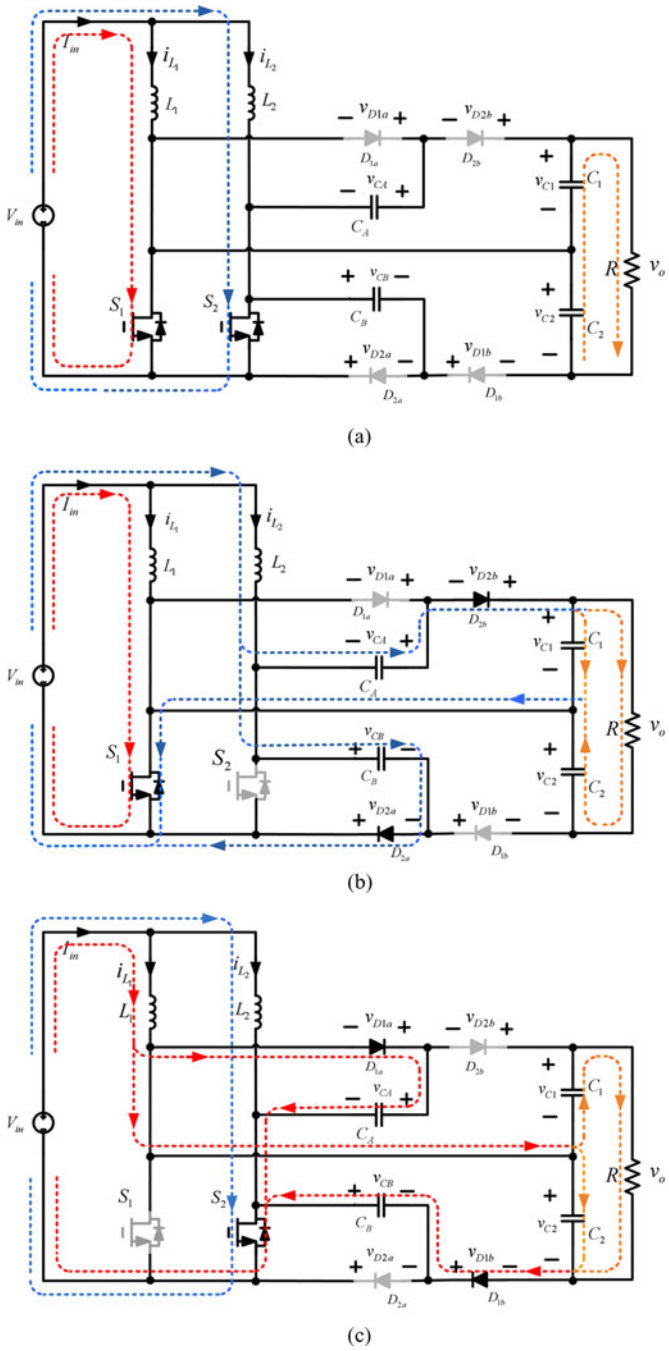

Fig. 3. Equivalent circuit of the proposed converter (a) Mode 1 and 3 (b) Mode 2 (c) Mode 4.

$$C_1 \frac{dv_{C_1}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R} \tag{5}$$

$$C_2 \frac{dv_{C_2}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R}. \tag{6}$$

Mode 2 ($t_1 \le t < t_2$): For this operation mode, switch S_1 remains conducting and S_2 is turned OFF. Diodes D_{2a} and D_{2b} become conducting. The corresponding equivalent circuit is shown in Fig. 3(b). It is seen from Fig. 3(b) that part of stored energy in inductor L_2 as well as the stored energy of C_A is now released to output capacitor C_1 and load. Meanwhile,

part of stored energy in inductor L_2 is stored in C_B. In this mode, capacitor voltage V_{C1} is equal to $V_{\rm CB}$ plus $V_{\rm CA}$. Thus, i_{L1} still increases continuously and i_{L2} decreases linearly. The corresponding state equations are given as follows:

$$L_1\frac{di_{L1}}{dt} = V_{\rm in} \tag{7}$$

$$L_2\frac{di_{L2}}{dt} = V_{\rm in} + v_{C_A} - v_{C_1} = V_{\rm in} - v_{C_B} \tag{8}$$

$$C_A\frac{dv_{C_A}}{dt} = i_{C_B} - i_{L_2} \tag{9}$$

$$C_B\frac{dv_{C_B}}{dt} = i_{C_A} + i_{L_2} \tag{10}$$

$$C_1\frac{dv_{C_1}}{dt} = -i_{C_A} - \frac{(v_{C_1}+v_{C_2})}{R} \tag{11}$$

$$C_2\frac{dv_{C_2}}{dt} = -\frac{(v_{C_1}+v_{C_2})}{R}. \tag{12}$$

Mode 3 ($t_2 \le t < t_3$): For this operation mode, as can be observed from Fig. 3, both S_1 and S_2 are turned ON. The corresponding equivalent circuit turns out to be the same as Fig. 3(a).

Mode 4 ($t_3 \le t < t_4$): For this operation mode, switch S_2 remains conducting and S_1 is turned OFF. Diodes $D_{1\rm a}$ and $D_{1\rm b}$ become conducting. The corresponding equivalent circuit is shown in Fig. 3(c). It is seen from Fig. 3(c) that the part of stored energy in inductor L_1 as well as the stored energy of C_B is now released to output capacitor C_2 and load. Meanwhile, part of stored energy in inductor L_1 is stored in C_A. In this mode, the output capacitor voltage V_{C2} is equal to $V_{\rm CB}$ plus $V_{\rm CA}$. Thus, i_{L2} still increases continuously and i_{L1} decreases linearly. The corresponding state equations are given as follows:

$$L_1\frac{di_{L1}}{dt} = V_{\rm in} - v_{C_2} + v_{C_B} = V_{\rm in} - v_{C_A} \tag{13}$$

$$L_2\frac{di_{L2}}{dt} = V_{\rm in} \tag{14}$$

$$C_A\frac{dv_{C_A}}{dt} = i_{C_B} + i_{L_1} \tag{15}$$

$$C_B\frac{dv_{C_B}}{dt} = i_{C_A} - i_{L_1} \tag{16}$$

$$C_1\frac{dv_{C_1}}{dt} = -\frac{(v_{C_1}+v_{C_2})}{R} \tag{17}$$

$$C_2\frac{dv_{C_2}}{dt} = -i_{C_B} - \frac{(v_{C_1}+v_{C_2})}{R}. \tag{18}$$

From the above illustration of the proposed converter, one can see that the operations of two-phase are both symmetric and rather easy to implement. Also, from key operating waveforms of the proposed converter is shown in Fig. 2. One can see the low voltage stress of two active switches and four diodes as well as the uniform current sharing.

III. Steady-State Analysis

In order to simplify the circuit performance analysis of the proposed converter in CCM, the same assumptions made in the previous section will be adopted.

A. Voltage Gain

Referring to Fig. 3(a) and (c), from the volt–second relationship of inductor L_1 (or L_2), one can obtain the following relations:

$$V_{\rm in}D + (V_{\rm in} - V_{\rm CA})(1-D) = 0 \tag{19}$$

$$V_{\rm in}D + (V_{\rm in} - V_{\rm CB})(1-D) = 0. \tag{20}$$

Also from the equivalent circuits in Fig. 3(b) and (c), voltage V_{C1} and V_{C2} can be derived as follows by substituting the $V_{\rm CA}$ and $V_{\rm CB}$ solutions of (19) and (20):

$$V_{C1} = V_{\rm CA} + V_{\rm CB} = \frac{2}{1-D}V_{\rm in} \tag{21}$$

$$V_{C2} = V_{\rm CA} + V_{\rm CB} = \frac{2}{1-D}V_{\rm in}. \tag{22}$$

It follows from (21) and (22) that the output voltage can be obtained as follows:

$$V_o = V_{C1} + V_{C2} = \frac{4}{1-D}V_{\rm in}. \tag{23}$$

Thus, the voltage conversion ratio M of the proposed converter can be obtained as follows:

$$M = \frac{V_o}{V_{\rm in}} = \frac{4}{1-D}. \tag{24}$$

B. Voltage Stresses on Semiconductor Components

To simplify the voltage stress analyses of the components of the proposed converter, the voltage ripples on the capacitors are ignored. From Fig. 3(b) and (c), one can see that the voltage stresses on active power switches S_1 and S_2 can be obtained directly as shown in the following equation:

$$V_{S1,\max} = V_{S2,\max} = \frac{1}{1-D}V_{\rm in}. \tag{25}$$

Substituting (23) into (25), the voltage stresses on the active power switches can be expressed as

$$V_{S1,\max} = V_{S2,\max} = \frac{V_O}{4}. \tag{26}$$

From (26), one can see that the voltage stress of active switches of the proposed converter is equal to one fourth of the output voltage. Hence, the proposed converter enables one to adopt lower voltage rating devices to further reduce both switching and conduction losses.

As can be observed from the equivalent circuits in 3(a) and (c), the open circuit voltage stress of diodes $D_{1\rm a}$, $D_{2\rm a}$, $D_{1\rm b}$, and $D_{2\rm b}$ can be obtained directly as shown in (27).

$$V_{D1a,\max} = V_{D1b,\max} = V_{D2b,\max} = \frac{V_O}{2}, V_{D2a,\max} = \frac{V_O}{4}. \tag{27}$$

In fact, one can see from (27) that the maximum resulting voltage stress of diodes is equal to $V_O/2$. Hence, the proposed converter enables one to adopt lower voltage rating diodes to further reduce conduction losses.

C. Characteristic of Uniform Input Inductor Current Sharing

By using the state space averaging technique, one can repeat the previous process to get the averaged state equations quite straightforward as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{\text{in}} - (1-D)V_{\text{CA}} \tag{28}$$

$$L_2 \frac{di_{L2}}{dt} = V_{\text{in}} - (1-D)V_{\text{CB}} \tag{29}$$

$$C_A \frac{dv_{\text{CA}}}{dt} = \frac{(1-D)C_A\left(C_{\text{eq1}}I_{L1}(C_2+C_B) - C_{\text{eq2}}I_{L2}C_1\right)}{C_{\text{eq1}}C_{\text{eq2}}} - \frac{(1-D)C_AC_B\left(C_{\text{eq1}}+C_{\text{eq2}}\right)(V_{C1}+V_{C2})}{C_{\text{eq1}}C_{\text{eq2}}R} \tag{30}$$

$$C_B \frac{dv_{\text{CB}}}{dt} = \frac{(1-D)C_B\left(C_{\text{eq2}}I_{L2}(C_1+C_A) - C_{\text{eq1}}I_{L1}C_2\right)}{C_{\text{eq1}}C_{\text{eq2}}} - \frac{(1-D)C_AC_B\left(C_{\text{eq1}}+C_{\text{eq2}}\right)(V_{C1}+V_{C2})}{C_{\text{eq1}}C_{\text{eq2}}R} \tag{31}$$

$$C_1 \frac{dv_{C1}}{dt} = \frac{(1-D)C_1\left(C_AI_{\text{L2}}R - (C_A+C_B)(V_{C1}+V_{C2})\right)}{C_{\text{eq1}}R} - \frac{D(V_{C1}+V_{C2})}{R} \tag{32}$$

$$C_2 \frac{dv_{C2}}{dt} = \frac{(1-D)C_2\left(C_BI_{\text{L1}}R - (C_A+C_B)(V_{C1}+V_{C2})\right)}{RC_{\text{eq2}}} - \frac{D(V_{C1}+V_{C2})}{R} \tag{33}$$

where $i_{L1}, i_{L2}, v_{\text{CA}}, v_{\text{CB}}, v_{C1}$, and v_{C2} denote the average state variables, $I_{L1}, I_{L2}, V_{\text{CA}}, V_{\text{CB}}, V_{C1}$, and V_{C2} represent the corresponding dc values. $C_{eq1} = C_1C_A + C_1C_B + C_AC_B$, $C_{eq2} = C_2C_A + C_2C_B + C_AC_B$, and $I_o = (V_{C1}+V_{C2})/R$.

By selecting $C_1 = C_2 = \text{C}_x$, $C_A = C_B = C_y$, one can get the corresponding dc solutions as follows:

$$I_{L1} = I_{L2} = \left(\frac{2}{1-D} + \frac{\text{DC}_y}{(1-D)C_x}\right) I_o. \tag{34}$$

From (34), one can see that the proposed voltage quadrupler indeed possesses the inherent automatic uniform current sharing capability.

D. Performance Comparison

For demonstrating the performance of the proposed converter, the proposed converter is compared with some recent high step-up converters introduced in [24]–[26] as shown in Table I.

Table I summarize the voltage gain and normalized voltage stress of active as well as passive switches for reference. As an illustration, Fig. 4 shows the corresponding characteristic curve of the proposed converter. For comparison, the voltage stress is normalized by the output voltage V_O, the voltage gains, the normalized switch stresses and the normalized output diode stresses of the conventional voltage-doubler [24], high step-up ratio converter [25], and the ultrahigh step-up converter [26] are also shown in the same figure to provide better view.

TABLE I
COMPARISON OF THE STEADY-STATE CHARACTERISTICS FOR FOUR CONVERTERS

Gain/stress	Voltage Doubler [24]	High step-up ratio converter [25]	Ultra high step-up converter [26]	Proposed converter
Voltage gain	$\frac{2}{(1-D)}$	$\frac{3-D}{(1-D)}$	$\frac{3+D}{(1-D)}$	$\frac{4}{(1-D)}$
Voltage stress of switches	$\frac{1}{2}$	$\frac{1}{(3-D)}$	$\frac{2}{(3+D)}$	$\frac{1}{4}$
Voltage stress of diodes	1	$\frac{2}{(3-D)}$	$\frac{2}{(3+D)}$	$\frac{1}{2}$
numbers of MOSFETs	2	2	1	2
numbers of inductors	2	2	2	2
numbers of diodes	2	3	5	4
numbers of capacitors	2	3	4	4

It is seen from Fig. 4(a) that the proposed converter can achieve higher voltage gain than that of the other three boost converters. Therefore, the proposed converter is rather suitable for use in applications requiring high step-up voltage gain. From Fig. 4(b), one can see that the proposed converter can achieve the lowest voltage stress for the active switches. Also, from Fig. 4(c), it is seen that the proposed converter can achieve the lowest voltage stress for the diodes. As a result, one can expect that with proper design, the proposed converter can adopt switch components with lower voltage ratings to achieve higher efficiency.

IV. Simulation and Experimental Results

To facilitate understanding the merits and serve as a verification of the feasibility of the proposed converter, a prototype with 25-V input, 400-V output, and 400-W rating is constructed as shown in Fig. 1 is chosen. The switching frequency is chosen to be 40 kHz, both duty ratios of S_1 and S_2 equal to 0.75 and the corresponding component parameters are listed in Table II for reference. Due to the low switch voltage stress of the proposed converter, two power MOSFETs rating of 150 V and conductive resistance of 13 mΩ, namely IXFH150N15P are adopted. Similarly, four diodes with low forward voltage drop, namely DSEP 60-025A are chosen.

The interleaved structure can effectively increase the switching frequency and reduce the input and output ripples as well as the size of the energy storage inductors. Fig. 5 shows the two-phase inductor current waveforms of the simulation and

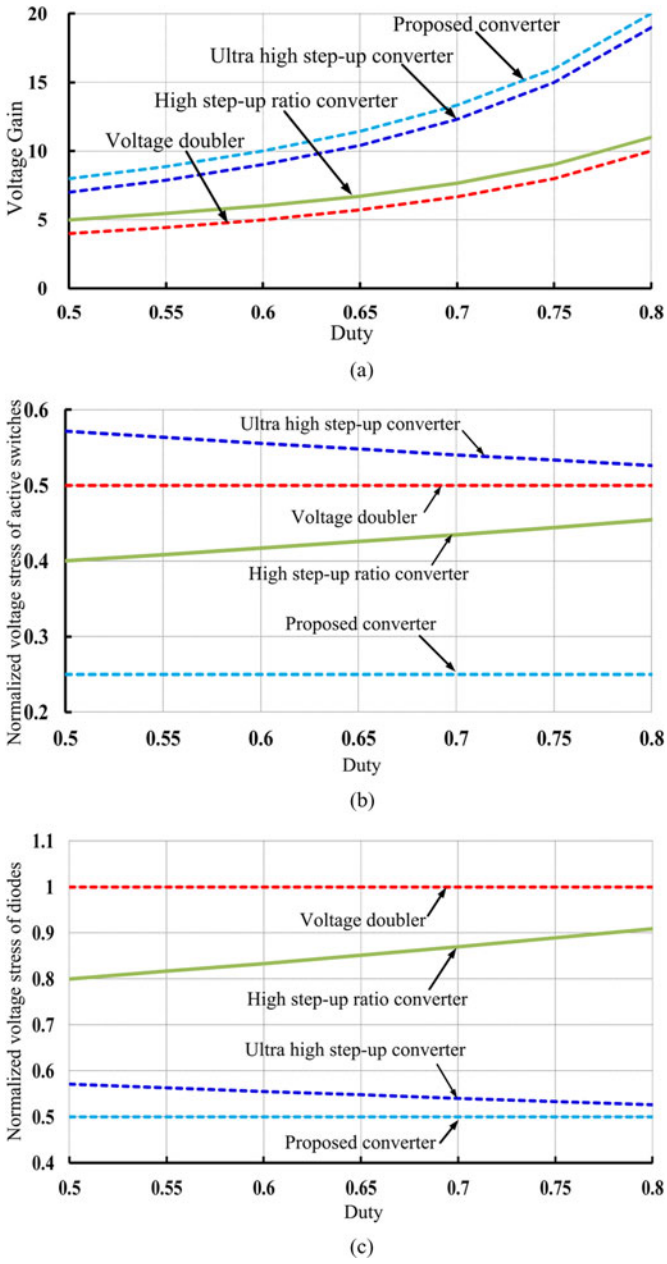

Fig. 4. Comparison of the steady-state characteristics for four different converters (a) voltage gain (b) normalized voltage stress of active switches (c) normalized voltage stress of diodes.

TABLE II
COMPONENT PARAMETERS OF THE PROTOTYPE SYSTEM

Components	Specification
Boost Inductors (L_1, L_2)	CH330060, 253μH
Active Switches (S_1, S_2)	IXFH150N15P, 150V, $R_{ds(on)}$=13mΩ
Blocking capacitors (C_A, C_B)	10uF/250V (R_c=4.6 mΩ)
Output capacitors (C_1, C_2)	250uF/250V (R_c=44 mΩ)
Power diodes (D_{1a}, D_{1b}, D_{2a}, D_{2b})	DSEP 60-025A

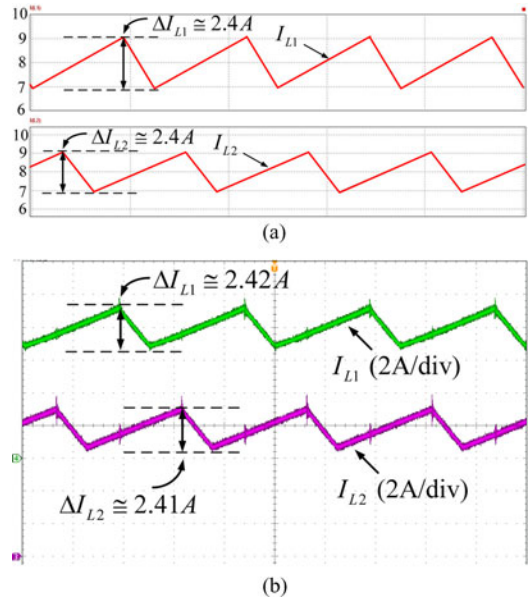

Fig. 5. Waveforms of inductors current I_{L1}, I_{L2} (a) simulation results (b) experimental results (10 μs/div).

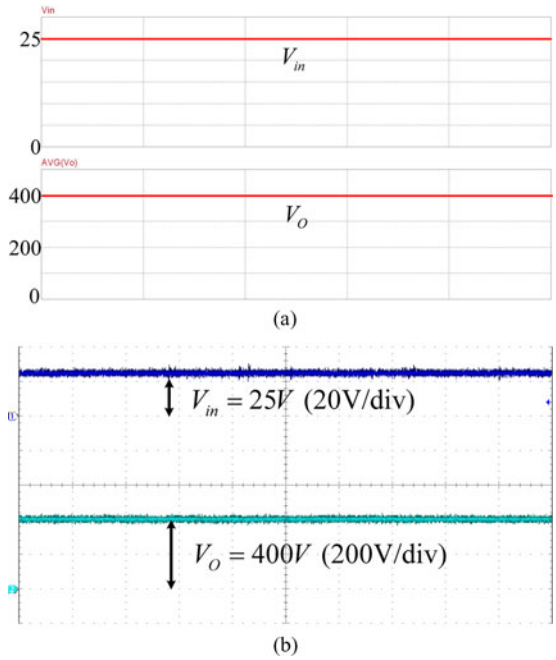

Fig. 6. Waveforms of input current and output voltage (a) simulation results (b) experimental results (10 μs/div).

experimental results. Both simulated inductor current ripples are about 2.4 A, while the experimental ones are about 2.41 A. Since input current I_{in} is equal to I_{L1} plus I_{L2}, it is obvious that with the two-phase interleaving control, both input current ripples and switch conduction losses can be reduced.

The simulation and experimental waveforms of the input and output voltages are shown in Fig. 6. The measured input voltage is 25 V, and the output voltage is 400 V.

To check the validity of the capacitor voltage stress, waveforms of output capacitors and blocking capacitors are recorded

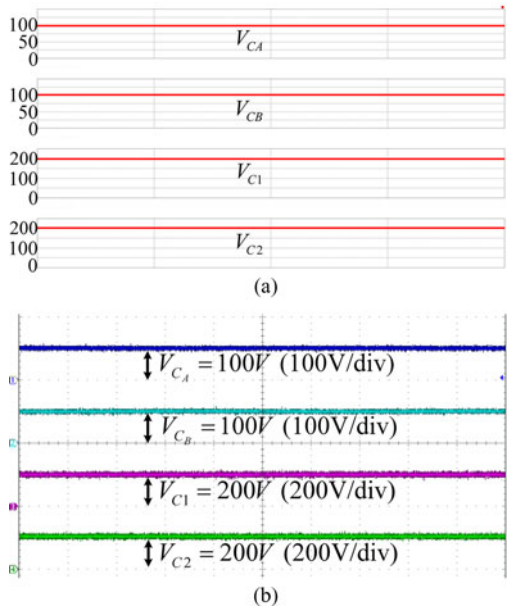

Fig. 7. Waveforms of the blocking capacitors and output capacitors voltages (a) simulation results (b) experimental results (10 μs/div).

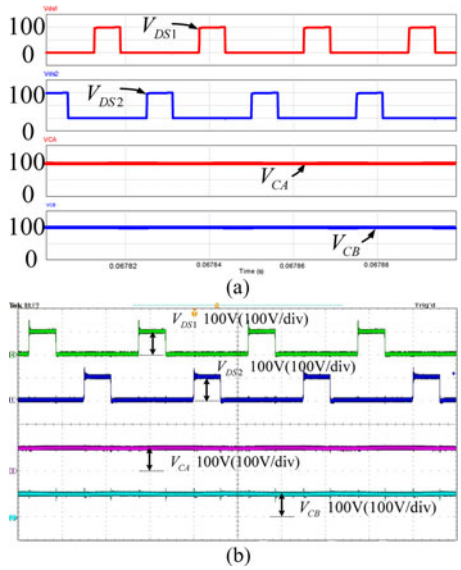

Fig. 8. Waveforms of the voltage stress of $V_{\mathrm{DS1}}, V_{\mathrm{DS2}}, V_{\mathrm{CA}}$, and V_{CB} (a) simulation results (b) experimental results (10 μs/div).

as shown in Fig. 7. From Fig. 7, one can see that, with the proposed converter, the voltage stresses of the output capacitors and blocking capacitors are indeed equal to one half and one fourth of the output voltage, respectively.

Similarly, to check the correctness of (26), experiments are made and the results are shown in Fig. 8. From Fig. 8, one can observe that the voltage stress of the active switches is equal to one fourth of the output voltage. Also, to check the voltage stress of blocking capacitors, one can see when the proposed converter is operated in modes 2 and 4, the voltages of capacitors C_A and C_B are clamped at $\frac{V_{\mathrm{in}}}{1-\mathrm{D}}$, and when the proposed converter is operated in modes 1 and 3, all diodes are OFF, and capacitors C_A and C_B are isolated as open circuits;

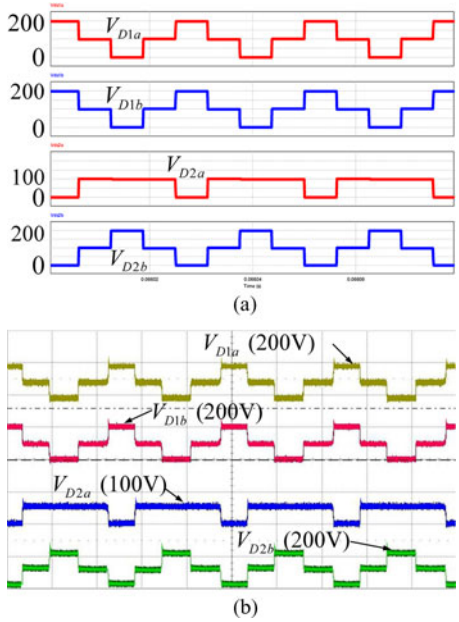

Fig. 9. Waveforms of the voltage stress of $V_{D1\mathrm{a}}, V_{D1\mathrm{b}}, V_{D2\mathrm{a}}$, and $V_{D2\mathrm{b}}$ (a) simulation results (b) experimental results (10 μs/div).

hence, the voltages of capacitors C_A and C_B are kept constant. Also, the output loading is mainly supplied by capacitors C_1 and C_2. Therefore, the voltages across C_A and C_B can be maintained at constant dc values even though C_A and C_B are with rather small capacitance.

The diode voltage waveforms of the simulation and experimental results are shown in Fig. 9, which indicates that the maximum voltage cross diodes $V_{D1\mathrm{a}}, V_{D1\mathrm{b}}$, and $V_{D2\mathrm{b}}$ equals 200 V which is indeed equal to one-half of the output voltage. The maximum voltage crosses diode $V_{D2\mathrm{a}}$ is 100 V which is equal to one fourth of the output voltage as expected.

The diode current waveforms of the simulation and experimental results are shown in Fig. 10. In the proposed topology, low-voltage-rating rectifier diodes are used to reduce the conduction loss. Due to the help of the blocking capacitor, the output current ripples are reduced.

A precise power meter (YOKOGAWA-WT3000) was used to measure the efficiency of the proposed converter. Fig. 11 shows the measured efficiency curve of the proposed high step-up converter. The measured full-load efficiency is 94.32% and the maximum efficiency is 96.05%. It can be seen that from Fig. 11, with the increase of the output load, the conversion efficiency decreases due to larger current which will result in relatively larger input-side conduction losses and switching losses.

Fig. 12 shows the corresponding loss analysis of the proposed converter at full load as an illustration. By analyzing the power losses distribution, it can be concluded that the major losses come from the active switches, the diodes, and the input inductors. From Fig. 12, it can also be seen that the conduction loss of diodes is obviously larger than other component losses. In order to further increase the converter efficiency, one can adopt the synchronous rectifier technology, namely replace four diodes with four MOSFETs. The corresponding measured efficiency

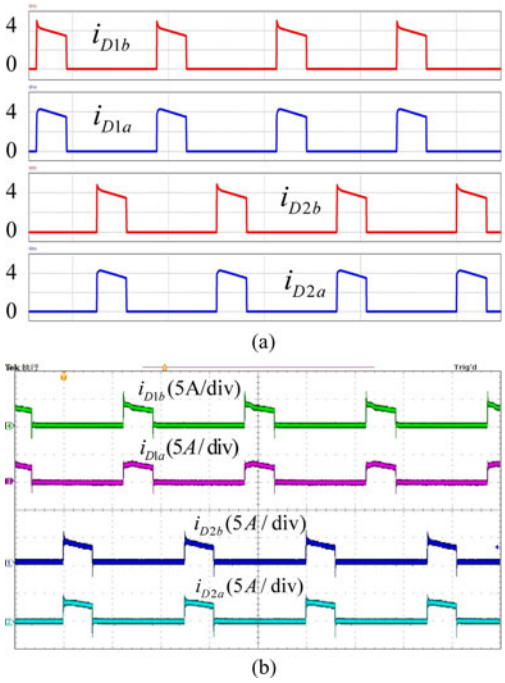

Fig. 10. Waveforms of the current of $i_{D1a}, i_{D1b}, i_{D2a}$, and i_{D2b} (a) simulation results (b) experimental results (10 μs/div).

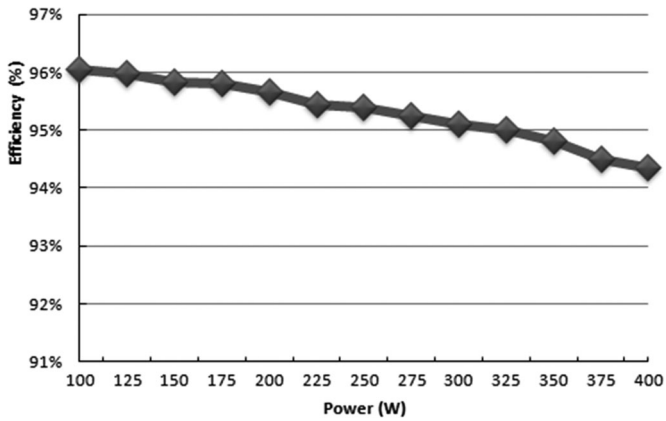

Fig. 11. Measured efficiency of the proposed converter.

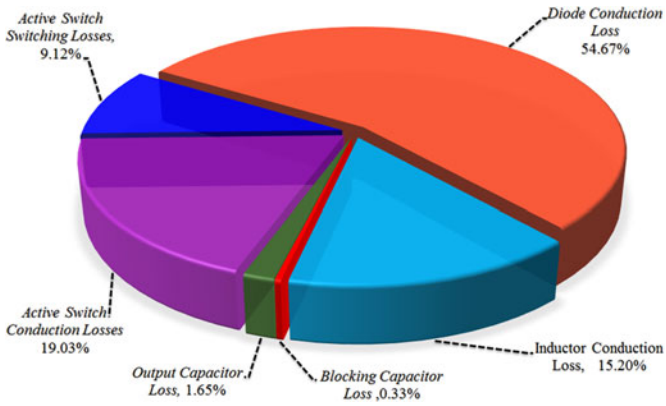

Fig. 12. Shows loss analysis of the proposed converter at full load.

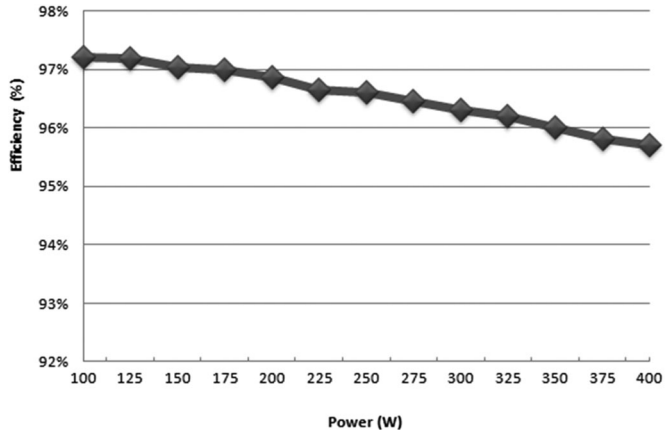

Fig. 13. Measured efficiency of the proposed converter with synchronous rectifier technology.

curve is shown in Fig. 13. From Fig. 13, it can be seen that the measured full-load efficiency of the proposed converter with synchronous rectifier is 95.67%, and the maximum efficiency is nearly 97.12%.

V. Conclusion

In this paper, a novel transformer-less adjustable voltage quadrupler dc–dc converter with high voltage transfer gain and reduced semiconductor voltage stress is proposed. The proposed topology utilizes input-parallel output-series configuration and is derived from a two-phase interleaved boost converter for providing a much higher voltage gain without adopting an extreme large duty cycle. The proposed converter cannot only achieve high step-up voltage gain but also reduce the voltage stress of both active switches and diodes. This will allow one to choose lower voltage rating MOSFETs and diodes to reduce both switching and conduction losses. In addition, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the two interleaved phases for voltage boosting mode without adding any extra circuitry or complex control methods. The operation principle and steady analysis as well as a comparison with other recent existing high step-up topologies are presented. Finally, a 400-W rating prototype with 25-V input and 400-V output is constructed for verifying the validity of the proposed converter. It is seen that the resulting experimental results indeed agree very close and show great agreement with the simulation results. Therefore, the proposed converter is very suitable for applications requiring high step-up voltage gain.

Appendix

According to the simulated and experimental voltage and current waveforms of the switches, diodes, inductors, and capacitors are adopted to calculate, the approximate loss of each component at full load and the results listed as following (A1)–(A6), for reference. Also, to simplify calculating, the converter losses, the voltage, and current waveforms are approximated

with piecewise linear segment. The corresponding expressions of losses are shown as follows.

A. Active Switch Conduction Losses

$$I_{S1(\mathrm{rms})}^2 \times R_{\mathrm{DS1(on)}} + I_{S2(\mathrm{rms})}^2 \times R_{\mathrm{DS2(on)}} = \left[\frac{I_{\mathrm{in}}^2}{18}(17-8D)\right] \times \left(R_{\mathrm{DS1(on)}} + R_{\mathrm{DS2(on)}}\right). \quad \text{(A1)}$$

B. Active Switch Switching Losses

$$\frac{1}{2}\times V_{\mathrm{DS}} \times I_{S(\mathrm{low})} \times T_r \times f_S + \frac{1}{2} \times V_{\mathrm{DS}} \times I_{S(\mathrm{peak})} \times T_f \times f_S = \frac{V_{\mathrm{DS}} I_{\mathrm{in}}}{4}(T_r + T_f) \times f_S + \frac{V_{\mathrm{DS}} V_{\mathrm{in}}}{8L}(2D-1)T_S\,(T_r - T_f) \times f_S. \quad \text{(A2)}$$

C. Diode Conduction Losses

$$\left(I_{D1a(\mathrm{avg})} + I_{D1b(\mathrm{avg})} + I_{D2a(\mathrm{avg})} + I_{D2b(\mathrm{avg})}\right) \times V_F + \left(I_{D1a(\mathrm{rms})}^2 + I_{D1b(\mathrm{rms})}^2 + I_{D2a(\mathrm{rms})}^2 + I_{D2b(\mathrm{rms})}^2\right) \times r_F = (1-D) \times I_{\mathrm{in}} \times V_F + \left(\frac{(1-D)I_{\mathrm{in}}^2}{4} + \frac{D(1-D)V_{\mathrm{in}}^2}{3f^2L^2}\right) \times r_F. \quad \text{(A3)}$$

D. Inductor Conduction Losses

$$R_{L1} \times I_{L1(\mathrm{rms})}^2 + R_{L2} \times I_{L2(\mathrm{rms})}^2 = (R_{L1} + R_{L2})\left[\frac{I_{\mathrm{in}}^2}{4} + \frac{DV_{\mathrm{in}}^2}{12L^2f^2}\right]. \quad \text{(A4)}$$

E. Output Capacitor Losses

$$R_{C1} \times I_{C1(\mathrm{rms})}^2 + R_{C2} \times I_{C2(\mathrm{rms})}^2 = (R_{C1} + R_{C2})\,\frac{D^2 I_{\mathrm{in}}^2}{16}(1-D). \quad \text{(A5)}$$

F. Blocking Capacitor Losses

$$R_{\mathrm{CA}} \times I_{\mathrm{CA(rms)}}^2 + R_{\mathrm{CB}} \times I_{\mathrm{CB(rms)}}^2 = (R_{\mathrm{CA}} + R_{\mathrm{CB}})\,\frac{I_{\mathrm{in}}^2}{8}(1-D). \quad \text{(A6)}$$

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