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Analysis of High Power Switched Capacitor Converter Regulation based on Charge-balance Transient-calculation Method

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***Abstract*—Switched Capacitor (SC) Converters were initially introduced for low power applications and monolithic integration. In recent years, SC converter has found high power applications. However, voltage regulation remains an issue. This paper addresses regulation challenges for high power SC converters, based on Charge-balance Transient-calculation (CT) modeling method and peak current stress estimation. With the help of CT model, due to its accuracy and comprehensive relationship, circuit and control parameters' impacts on regulation become straightforward and concerns on components stresses can be addressed quantitatively. The suitability of CT method for regulation analysis is confirmed by comparison with traditional modeling methods. The CT method is used in a 1kW 3X Two-switch Boosting Switched-capacitor Converter (TBSC) circuit for steady state analysis and current stress estimation. The soft rising input current and nature interleaving properties of 3X TBSC make it well-suited for high power application. Finally, the small signal model of the 3X TBSC is developed and a closed loop operation is achieved under 1kW power rating.**

***Index Terms*— CT modeling, switched capacitor, voltage regulation, peak current stress, TBSC**

I. INTRODUCTION

Since 1990s, Switched Capacitor Converter(SCC) has attracted attentions from power electronics community due to its unique property: no participation of magnetic components[1]–[3]. This special characteristic enables it to target at higher power density and full monolithic integration compared with traditional inductor-based converter[4]–[7]. However, it also brings the issues of narrowed regulation capability and pulsating input current[8]–[10].

In the past, regulation of SCC was mostly investigated under low power applications from several milli-watts to tens of watts, using Pulse Width Modulation(PWM) method, Frequency Modulation(FM) method[11], [12] or combination of them[13]. Meanwhile, new methods were proposed to overcome the pulsating input current and widen the line-load regulation range. One typical method to eliminate pulsation input current is to control the gate voltage [14], [15]. This method suggests not to fully turn-off the switch that is connected at input. Instead, it controls the switch as "Quasi-switch" and uses the "saturation" region of the switch to regulate the output voltage. Since the switch is operated as a voltage controlled current source, certain amount of voltage drop on the drain-source of the switch causes undesirable losses. Another method that adopted adaptive mixed-on time and switching frequency control was proposed in [16], in which several switched-capacitor branches were interleaved and the calculated "on time" is "merged" together to achieve seamless charging from input source, thus continuous input current is expected. However, the control is complicated and the risk of "overlap" or "underlap" interleaving is high. Besides, large amount of components are required to achieve this control strategy. In this paper, instead of pursuing absolute continuous input current, soft rising input current with the aid of Coupling-Switched-Capacitor (CSC) Loops is discovered. Compared with the traditional spiky input current, the reduced di/dt at input current could alleviate EMI emission to the input source and is more desirable for high power SCC applications.

When it comes to high power SC converters, unregulated control is a common control strategy [17], [18]. The reason may come from the concerns on the added loss due to regulation and also the challenges of component stress by lack of optimization design guidance. Some researchers introduced inductive elements along the charging or discharging loops to change the SC converter to resonant SC converter and mitigate the current pulsation[19], [20]. Attempt to regulate high power SC converter was rarely seen in literatures. A regulation analysis for high power SCC with inductive element was given in paper [21], but a remedy for the "cut off" stress caused by inductive element is still needed. The introduction of inductive element seems helpful to suppress the peak current and improve system efficiency for high power applications, since soft switching condition can be intentionally created. However, further investigation of SCC model reveals that it may not always be the case, especially when the SC is operating in high switching frequency.

In a typical SC converter charging loop show as Fig. 1(a), the circuit charging current waveforms under different frequency conditions were derived in paper [22], [23], described as Fig. 1(b). If a resonant tank is created along the

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charging loop by adding an inductor Ls, a possible charging current can be derived as Fig. 1(c), under zero damping factor condition[21]. It can be seen when the same amount of charge is delivered during equal period of Ti, the resonant charging approach may not always maintain lowest peak current. Moreover, the regulation under resonant operation is more difficult, considering the inductor current tending to continue. Therefore, the advantage of introducing resonance to SC converter for high power SC converter with regulation capability is still plausible.

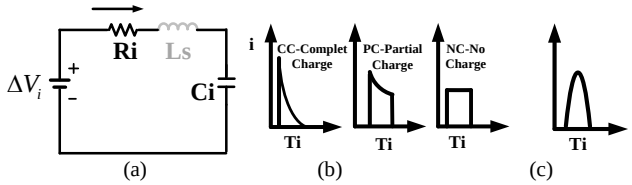

Fig. 1. Charging current (a) Charging loop (b) Charging current under different frequency conditions (c) Charging current with resonant inductor

In this paper, analysis on high power SC converter regulation will be conducted. A proper mathematics modelling method for SC converter regulation analysis is in critical demand. For this purpose, many modeling methods for SCC were evaluated[23]–[30].However, most models adopted energy conservation or current averaging estimation, which may not be able to predict the transient behavior of circuit, which is critical for component selection.

The primary objective of this paper is to explore proper modeling method for SC converter and provide systematic analysis to address the regulation issue on high power SCC. The rest of paper is organized as follows: the Charge-balance Transient-calculation(CT) modeling method[16], [28] is investigated in section II. Its accuracy is confirmed by comparison with traditional modeling methods. The peak current stress is derived based on CT method, which exhibits the component stress challenge of regulation for high power application. The suppression method of peak current is discussed. In section III, this method is applied to a 3X TBSC converter. The steady state model is obtained and the peak current formulas are provided. The mechanism of soft rising input current of 3X TBSC is analyzed, which suggests its suitability for high power application. The small signal model is developed for close loop design of 3X TBSC in section IV. In section V, simulation confirms the accuracy of CT method the peak current estimation. Experimental results demonstrate the feasibility of regulation for high power SCC.

II. Model Consideration for High Power SC Converter Regulation Analysis

In order to predict the transient behavior of high power SCC, a proper circuit model should be adopted for circuit analysis. It must be able to address the component stress and provide guidance for parameter optimization.

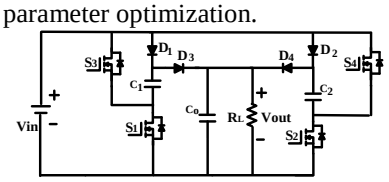

Fig. 2. A voltage doubler topology proposed in [32]

A. SCSSA modeling

In this section, Switched capacitor State Space Averaging(SCSSA) method, which simply adopted the state space averaging method[31] developed for PWM converters is reviewed, based on an typical voltage doubler circuit proposed in paper [32], shown as Fig. 2. According to the SCSSA method introduced in paper [32], the voltage gain formula of topology in Fig. 2 can be calculated as following:

$$\frac{V_o}{V_{in}-V_d}=\frac{2}{1+(1+\frac{1}{2d})\frac{r+R_{on}}{R_L}} \quad (1)$$

Where V_d is the voltage drop of all diodes, r is ESR of flying capacitor C_1 and C_2, R_{on} is the "on resistance" of all switches. Equation (1) demonstrates that the voltage gain can be regulated by control parameter d. At the same time, the gain curve will be affected by loop resistance $r + R_{on}$ and the load R_L.

The original SSA method was developed for conventional inductor-based PWM converter, having become industrial standard method for those converters. Nevertheless, simply adoption of it for SC converter analysis may not be adequate to describe the steady state at. For example, the gain equation is unable to explain the frequency regulation which has been reported frequently in SCC[11], [33]. Moreover, the impact of flying capacitor C_1 and C_2 is not observed. It is critical to establish comprehensive understanding of switching capacitor converter including the frequency regulation and flying capacitor effects on the voltage gain, especially when considering high power regulation condition.

B. Charge balance-Transient calculation(CT) Modeling Method

Alternatively, the voltage gain of circuit in Fig. 2 can be derived based on CT modeling method. The original idea of this method can be found in paper [16], [28], [34], but with different emphasizes. Paper [16] was focused on deriving the expression of "on time" in order to achieve adaptive control. Paper [28], [34] didn't adopt the linear discharging approximation for flying capacitors during discharging phase which makes the resulted equation complex. This paper constructs some extensive work on top of them and pursuits the regulation and stress analysis based on CT model. Moreover, the CT method is elaborated with standard procedures for voltage gain derivation.

Some assumptions are made here for calculation simplification: (1)All switches have identical on resistance R_{on}. (2)Flying capacitors C_1 and C_2 have the same capacitance C and Equivalent Series Resistance (ESR) r. (3)All diodes have the same voltage drop V_d. (4)The output current is assumed constant at flying capacitor discharging phase.

The steps of deriving SC converter voltage ratio are given as following:

1) Transient calculation

The only charging time for C_1 in one switching cycle is [0, dT_s], shown in Fig. 3(a). The voltage of C_1 rises from V_{c1min} to V_{c1max}, as shown in Fig. 4. By solving the differential equation based on the charging loop of C_1, it can be derived that:

$$V_{c1\max}=(V_{c1\min}-V_{in}+V_d)\,e^{-\frac{dT_s}{(r+R_{on})C}}+V_{in}-V_d \quad (2)$$

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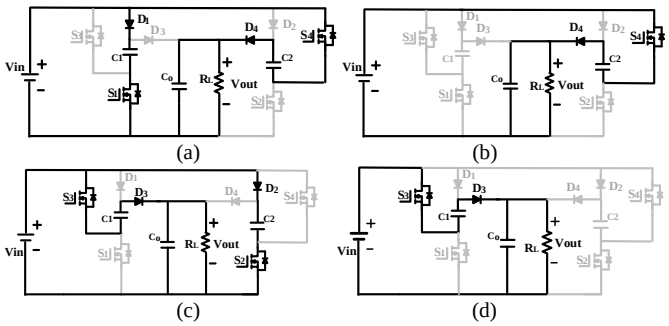

Fig. 3. Operation modes based on SSA method. (a) State1 [0, dT_s]. (b) State2 [dT_s, $\frac{dT_s}{2}$]. (c) State3 [$\frac{T_s}{2}$, dT_s+ $\frac{T_s}{2}$]. (d) State4 [dT_s+ $\frac{T_s}{2}$, T_s].

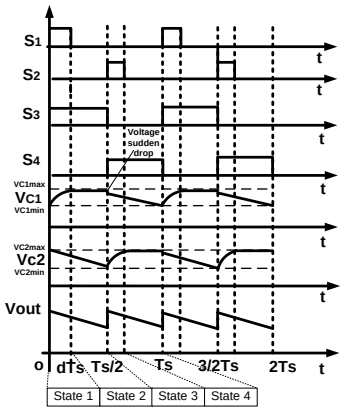

Fig. 4. Transient waveforms based on CT modeling method

2) Charge balance principal

The discharging period of C_1 are shown as Fig. 3(c) and (d) in one switching cycle. The voltage of C_1 decreases from V_{c1max} to V_{c1min}. The discharging current is assumed constant and equals to load current. According to charge balance principal, the following equation is got:

$$C_1(V_{c1\max} - V_{c1\min}) = \frac{V_{out} T_s}{2R_L} \tag{3}$$

3) Averaging output voltage

Due to the symmetrical configuration, flying capacitors C_1 and C_2 possess complementary charging and discharging procedures and the voltage of V_{c1} and V_{c2} have the same maximum and minimum values. The waveform of output voltage is depicted at the bottom of Fig. 4. Thus the average output voltage can be presented as:

$$V_{out} = V_{in} - V_d - \frac{V_{out}}{R_L}\left(R_{on} + r\right) + \frac{V_{c1\min} + V_{c1\max}}{2} \tag{4}$$

According to equations (2),(3),(4), the voltage ratio between input and output is derived as following:

$$\frac{V_{out}}{V_{in} - V_d} = \frac{8CR_L(e^{-\frac{dT_s}{RC}} - 1)}{4CR_L e^{-\frac{dT_s}{RC}} + 4CRe^{-\frac{dT_s}{RC}} - T_s e^{-\frac{dT_s}{RC}} - 4CR_L - 4CR - T_s} \tag{5}$$

Where R = R_{on} + r.

C. Comparison of SCSSA Model and CT model

In order to examine the differences between the aforementioned two modeling methods, equation (5) is rearranged as:

$$\frac{V_{out}}{V_{in} - V_d} = \frac{2R_L}{R_L + R + \frac{T_s}{4C}\frac{1}{\tanh(\frac{dT_s}{2RC})}} \tag{6}$$

Meanwhile, the formula (1) based on the traditional SSA modeling method is rearranged as:

$$\frac{V_o}{V_{in} - V_d} = \frac{2R_L}{R_L + R + \frac{1}{2d}R} \tag{7}$$

Where R = R_{on} + r.

Under the condition of dTs<<2RC, $\coth(\frac{dT_s}{2RC}) \approx \frac{dT_s}{2RC}$. The equation (6) approaches (7). Note that CT model contains two more parameters in the gain equation: the switching period T_s and flying capacitance C. Therefore, it can provide the intrinsic mechanism of frequency regulation and reveal the flying capacitor impact on voltage gain, which is not mentioned in the traditional SSA modeling method.

A gain comparison between SSA model and CT model is given as Fig. 5, where the simulation result is presented as a series of dots. The circuit and control parameters in Table I are adopted for model calculation and simulation.

TABLE I

CIRCUIT AND CONTROL PARAMETERS FOR MODEL COMPARISON

Fig. 5	V_{in} (V)	d	f_s (Hz)	Ron (Ω)	R (Ω)	C_1 (uF)	C_o (uF)	R_L (Ω)
(a)	5	0~0.5	4k, 10k, 100k	0.077	0.02	94	1	10
(b)	5	0~0.5	100k	0.077	0.02	5,10 94	1	10

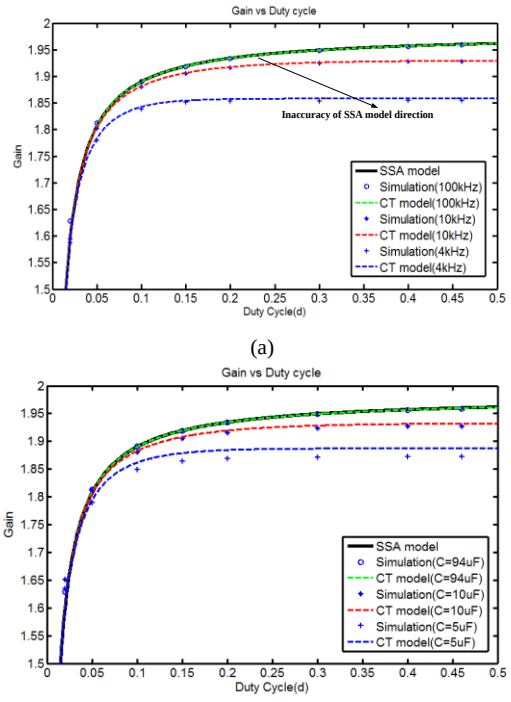

Fig. 5. Duty cycle regulation curves with different control parameters (a) Frequency effect (b) Flying capacitor effect

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For the SSA model, only loop resistance (R_{on}, r), duty cycle and load are involved in the final voltage gain equation. Therefore, only one regulation curve is plotted in Fig. 5(a) and (b), regardless of frequency and flying capacitor variation of the circuit. It coincides with the CT mode and the simulation result under 100kH switching frequency and 100uF flying capacitor condition.

Nevertheless, the simulation results in Fig. 5(a) show that when the frequency is decreased, the regulation curve tends to move "downward", which agrees well with the prediction of the CT method. While in Fig. 5(b), when the capacitance of flying capacitor is reduced, the lower voltage gain is also observed in simulation. The CT modeling result again agrees pretty well with this trend except a slight deviation under the condition of 5uF flying capacitance. This is because when C=5uF and Co=1u, there will be an obvious "voltage sudden drop" of C_1 (C_2) when S_3 (S_4) is turned on due to charge redistribution between C_1 (C_2) and Co. However, the model assumes the voltage of C_1 (C_2) starts to drop immediately at a constant rate when S_3 (S_4) is turned on. Therefore, in order to guarantee the accuracy of CT model, the condition of C>>Co is required, which leads the "voltage sudden drop" to be negligible. According to the comparison, the traditional SSA method is demonstrated to be too coarse to describe the voltage conversion ratio under the conditions of low switching frequency and small flying capacitance.

D. Model Selection for High Power SC converter Analysis

In order to provide more physical insights of circuit parameter effects on circuit behavior, the output impedance based on different modeling methods is explored. According to a comprehensive SC circuit model in Fig. 6 , the steady state equivalent circuit of Fig. 2 can be interpreted as m=1 and n=2. The output impedance Re using CT modeling can be derived as following by inspection of equation (6):

$$R_e = R + \frac{T_s}{4C}\coth\left(\frac{dT_s}{2RC}\right) \tag{8}$$

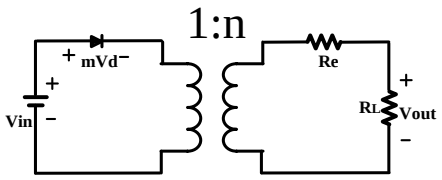


Fig. 6. Model of an idealized SCC

Similarly, based on the gain equation (7) obtained by SSA method, the correspondingly output impedance can be found as:

$$R_e = R + \frac{R}{2d} \tag{9}$$

Where R = R_{on} + r.

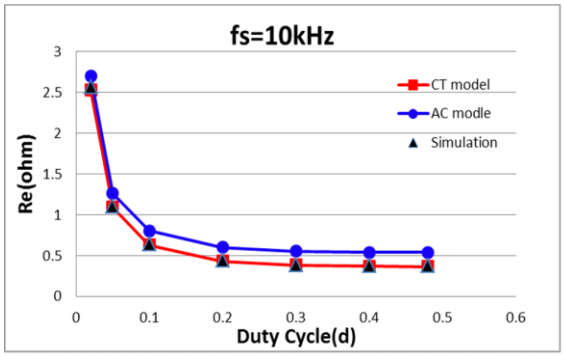
For comparison purpose, the modeling methods proposed in paper [23] and [24] recently are also applied to the converter in Fig. 2 and the corresponding output impedances are derived in Table II.

TABLE II

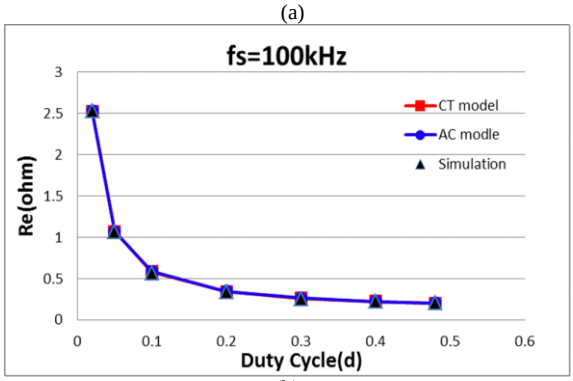
COMPARISON OF OUTPUT IMPEDANCE BASED ON DIFFERENT MOLDING METHOD

	Modeling methods	Output equivalent impedance
(a)	State Space Averaging(SSA) Model[32]	$R+\frac{R}{2d}$
(b)	Charge balance-Transient Calculation(CT) Model	$R+\frac{T_s}{4C}\coth(\frac{dT_s}{2RC})$
(c)	Average-current based Conduction loss(AC) Model[23]	$\frac{T_s}{4C}\coth(\frac{dT_s}{2RC})+\frac{T_s}{4C}\coth(\frac{T_s}{4RC})$
(d)	Slow and Fast Switching Limit(S-FSL) Model[24]	SSL Impedance: $\frac{T_s}{2C}$ FSL Impedance: $\frac{R_{on}}{2d}+R_{on}$

It can be seen different modeling methods have different emphasizes and limitations. The SSA method focuses on duty cycle regulation. This model is only accurate under small "on time" and large flying capacitance condition. The AC method reflects the duty cycle and frequency effects on the output impedance, but due to the loss estimation through average current, the accuracy under low switching frequency is impaired. However, under high frequency condition, the output impedance based on this method becomes the same as CT method, as the second item of output impedance in Table II(c) will evolve to R. A brief output impedance comparison between AC and CT methods is given under switching frequency at 10k and 100 kHz, in contrast with simulation results in Fig. 7. The other circuit parameters are set as Table I(a) for simulation and model calculation.



(a)



(b)

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Fig. 7. Comparison of CT model and AC model with simulation at different switching frequencies(a) fs=10kHz (b)fs=100kHz

For S-FSL method, it only emphasizes the impedance under very low frequency and very high frequency conditions. It is based on the energy conservation principal and neglects the duty cycle regulation effect. Moreover, the fast switching limit (FSL) doesn't consider the conduction loss of ESR of flying capacitors.

In view of above discussion, the CT modeling method provides more accurate prediction of circuit behavior under continuous variation of duty cycle and frequency conditions. Therefore, it's more suitable for high power SC converter analysis which demands more details in circuit transient analysis.

E. Peak Current Stress Model for High Power SCC

High power SC converters are very sensitive to circuit and control parameters, due to the possible high current stress. Since no inductive element is present, the risk of switch overshoot voltage for conventional inductor-based converter is mitigated. Therefore, the transient current stress of semiconductor components becomes the critical concern when applying the SC converters to high power area.

Topology in Fig. 2 is adopted to explore the transient current of SCC and its suppressing method.

1) Current transient at charging stage

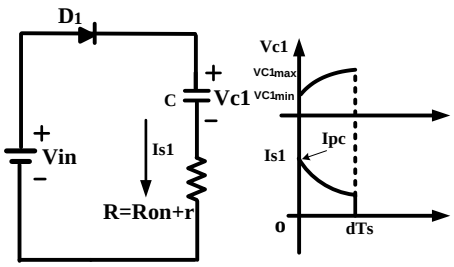

Fig. 8. Charging Phase

When the switch S_1 is turned on, according to charging loop shown as Fig. 8, the differential equation can be derived:

$$V_{in} - V_d - RC\frac{dV_{c1}(t)}{dt} - V_{c1}(t) = 0 \tag{10}$$

Because $V_{c1}(0) = V_{c1\min}$, the switch transient current is derived as following:

$$I_{s1}(t) = \frac{V_{in} - V_d - V_{c1\min}}{R} e^{-\frac{t}{CR}} \tag{11}$$

According to (2), (3), (4) derived in previous section, the expression of $V_{c1\min}$ can be derived as following:

$$V_{c1\min} = \frac{4C(1-e^{-\frac{dT_s}{CR}})(R+R_L) + T_s e^{-\frac{dT_s}{CR}} - 3T_s}{4C(1-e^{-\frac{dT_s}{CR}})(R+R_L) + (1+e^{-\frac{dT_s}{CR}})T_s}(V_{in} - V_d) \tag{12}$$

Therefore, the peak current for semiconductor S_1 (D_1) can be derived:

$$I_{pc} = I_{s1}(0) = \frac{4T_s}{4C(1-e^{-\frac{dT_s}{CR}})(R+R_L) + (1+e^{-\frac{dT_s}{CR}})T_s}\frac{V_{in} - V_d}{R} \tag{13}$$

To illustrate the peak current stress control method, the switch "on time" dT_s can be assumed to be a constant K for simplification purpose. If the peak charging current must be limited within ∂I_o, the switching frequency should satisfy following expression by rearranging equation (13) :

$$f_{s\_ch} > \frac{-\partial\left(1+e^{-\frac{K}{CR}}\right)I_o R + 4(V_{in} - V_d)}{4\partial C\left(1-e^{-\frac{K}{CR}}\right)I_o R(R+RL)} \tag{14}$$

It can be concluded that the peak current stress for SC converter is not always large even without participation of the stray inductance alone the circuit loops. Generally, the current stress is closely related with the duty cycle and switching frequency, when other circuit parameters are fixed. Lower switching frequency and smaller duty cycle can increase the peak current in the charging loop.

2) Current transient at discharging stage

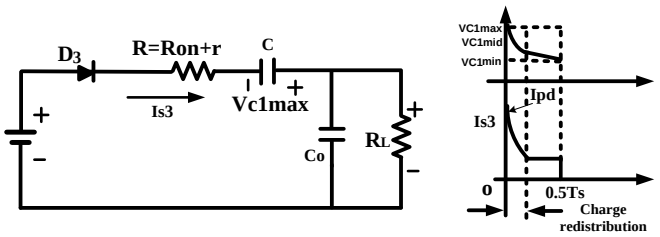

Fig. 9. Discharging Phase

At discharging stage of flying capacitor, the charge redistribution effect[27] between flying capacitor and output capacitor can cause large current spike. The voltage waveforms of flying capacitor C_1 and switch current are both presented in Fig. 9. To derive the peak current at this state, the differential equations are derived as following:

$$\begin{cases} V_{in} - V_d + RC\dfrac{dV_{c1}(t)}{dt} + V_{c1}(t) - V_{c0}(t) = 0 \\ C\dfrac{dV_{c1}(t)}{dt} = -C_o\dfrac{dV_{c0}(t)}{dt} - \dfrac{V_{out}}{R_L} \end{cases} \tag{15}$$

The initial state are: $V_{c1}(0) = V_{c1\max}, V_{co}(0) = V_{in} + V_{c1\min}$.

The switch transient peak current of S_3 (D_3) at discharging state can be derived as following:

$$I_{pd} = \frac{V_{c1\max} - V_{c1\min}}{R} = \frac{4T_s(1-e^{-\frac{dT_s}{CR}})}{4C(1-e^{-\frac{dT_s}{CR}})(R+R_L) + (1+e^{-\frac{dT_s}{CR}})T_s}\frac{V_{in} - V_d}{R} \tag{16}$$

According to equation (16), the circuit parameters such as flying capacitance and loop resistance and load can affect the discharging peak current.

Similar to peak charging current suppression method, if the peak discharging current is limited by βI_o, the switching frequency should be constrained by following inequality based on (16):

$$f_{s\_dis} > \frac{-\beta\left(1+e^{-\frac{K}{CR}}\right)I_o R + 4(1-e^{-\frac{K}{CR}})(V_{in} - V_d)}{4\beta C\left(1-e^{-\frac{K}{CR}}\right)I_o R(R+RL)} \tag{17}$$

Therefore, the system switching frequency should be designed as following:

$$f_s = \max\{f_{s\_ch}, f_{s\_\text{dis}}\} \tag{18}$$

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The above analysis procedure can also be applied to other two-stage SC converter. It is useful for high power SC converter design and parameter optimization.

III. ANALYSIS FOR HIGH POWER 3X TBSC

In order to further verify the CT modeling method and achieve certain regulation in high power condition, it is applied to a 3X TBSC converter to derive the voltage ratio. 3X TBSC is a member of Two-switch Boosting Switched-capacitor Converter(TBSC) family proposed in paper [35], shown in Fig. 10.It has some important characteristics preferable for high power application.

A. 3X TBSC topology

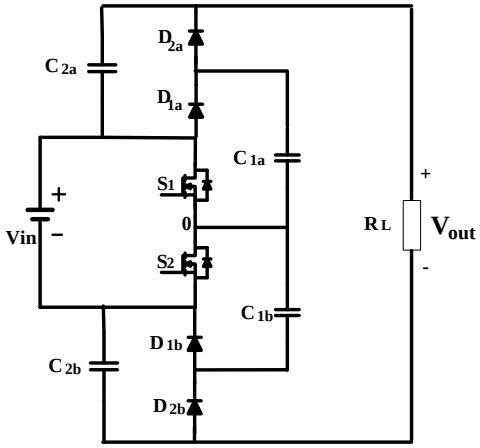

Fig. 10. Topology of 3X TBSC

This converter is naturally interleaved with only two active switches and its voltage gain is up to three times. The operation modes are given in Fig. 11. When only S_1 is turned on, input source will charge flying capacitor C_{1b}. At the same time, capacitor C_{1a} will charge capacitor C_{2a}. Both loops share the same path that contains the switch S_1, as shown in Fig. 11 (a). When only S_2 is turned on, V_{in} will charge C_{1a} while C_{1b} delivers energy to C_{2b}, shown in Fig. 11 (c). When S_1 and S_2 are both turned off, C_{2a} and C_{2b} will be connected in series with input source to power the load, partially serving as filter capacitor, shown as Fig. 11 (b) and Fig. 11 (d). Thus the input voltage is boosted.

B. Modeling of 3X SC converter using CT method

To simplify the voltage gain derivation of 3X TBSC, following assumptions are made: (1) Assume the load current is constant at C_{2a} discharging stage which is V_o/R_L (2) Assume all intermediate capacitors have the same capacitance C_{1a}=C_{1b}=C_{2a}=C_{2b}=C. (3) Assume all switches have the same "on resistance" R_{on} and all diodes have the same voltage drop V_d with diode resistance neglected (4) ESR of capacitors C_{2a} and C_{2b} is neglected for its partially filter functionality. Voltage gain derivation process is described out as following:

1) Transient calculation:

State 3 in Fig. 11(c) is the only state that C_{1a} is charged, thus the voltage of C_{1a} rises from its minimum value V_{c1amin} to maximum value V_{c1amax}. The transient equation based on KVL can be derived as following:

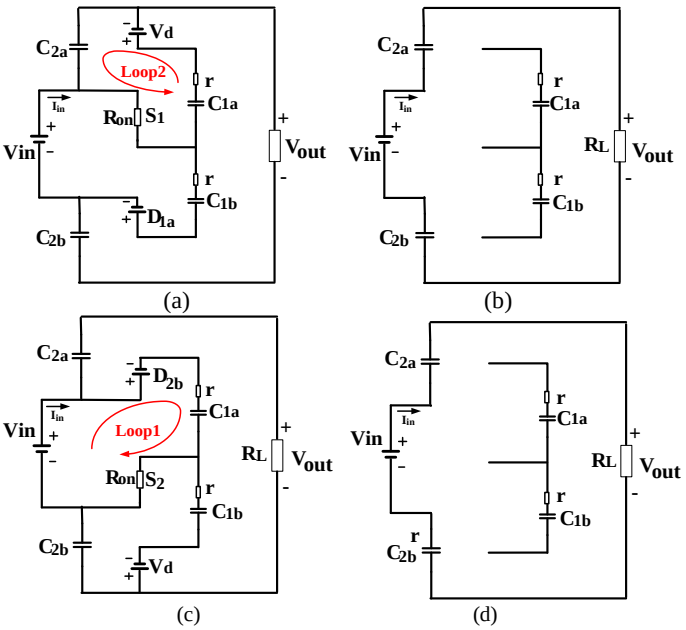

Fig. 11. Operation modes of 3X TBSC (a) State 1 [0, dT_s] (b) State 2 [dT_s, $\frac{T_s}{2}$] (c) State 3 [$\frac{T_s}{2}$, $dT_s+\frac{T_s}{2}$] (d)State 4 [$dT_s+\frac{T_s}{2}$, T_s]

$$V_{in}-V_d-R_1C\frac{dV_{c1a}(t)}{dt}+V_{c1a}(t)=0 \qquad (19)$$

where R_1 is the equivalent loop resistance of loop 1. R_1=r+kR_{on} and k is the effect coefficient of R_{on} caused by its coupling loop. It's obvious diodes D_{1a} and D_{2b} have the same average current which is equal to load current. Therefore, the voltage drop on R_{on} caused by the coupled loops can be approximated to be the same. Thus the effect coefficient k equals to 2. The decoupling procedure is shown as Fig. 12(a), where equivalent loop resistance R_1= r+2R_{on} is obtained. Similarly, the decoupling of loop 2 is given in Fig. 12(b) with derived loop resistance R_2= r+2R_{on}.

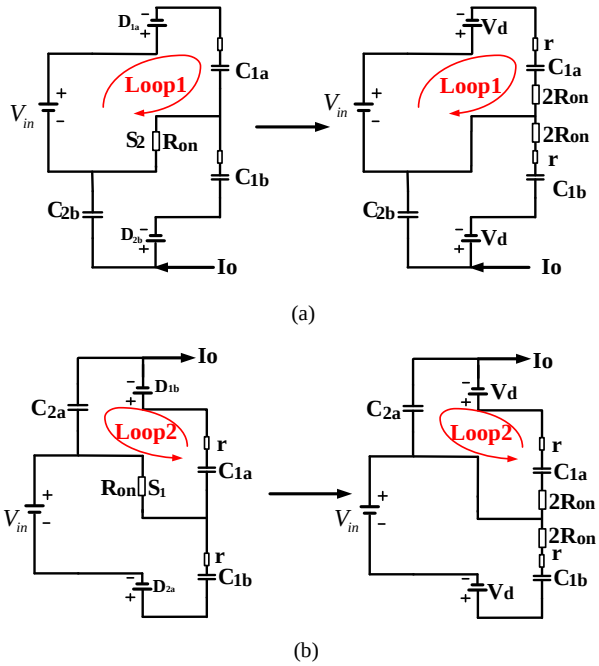

Fig. 12. Loop decoupling (a)Decoupling of loop 1 (b) Decoupling of loop 2

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Due to duration of State 3 is dT_s, the following relationship can be derived by solving differential equation (19):

$$V_{c1a\max} = V_{in} + e^{-\frac{dT_s}{R_1 C}}(V_{c1a\min} - V_{in} + V_d) - V_d \quad (20)$$

State 1 in Fig. 11 (a) is the only charging state for C_{2a}. So the voltage across C_{2a} rises from V_{2amin} to V_{2amax} at this time interval. The transient equation along loop 2 in Fig. 12(b) is given as following:

$$V_{c2a}(t) + V_d - R_2 C\frac{dV_{c1a}(t)}{dt} - V_{c1a}(t) = 0 \quad (21)$$

Where $R_2=r+2R_{on}$. Meanwhile, the following equation can be derived:

$$C(\frac{dV_{c1a}(t)}{dt} + \frac{dV_{c2a}(t)}{dt}) = -I_o \quad (22)$$

Where $I_o=V_{out}/R_L$. Solving the differential equations of (21),(22), it can be derived that:

$$V_{c2a\max} = \frac{V_{c1a\max} + V_{c2a\min} - V_d - \frac{I_o R_2}{2} - \frac{I_o dT_s}{C}}{2} - \frac{V_{c1a\max} - V_{c2a\min} - V_d - \frac{R_2 I_o}{2}}{2} e^{-\frac{2dT_s}{CR_2}} \quad (23)$$

2) Charge balance principal:

Since all the charge delivered to load will be first stored in intermediate flying capacitor C_{1a} during each switching period, the following equation based on the charge balance principal can be derived:

$$C(V_{c1a\max} - V_{c1a\min}) = I_o T_s \quad (24)$$

For filter capacitor C_{2a}, its voltage drops from maximum to minimum during state 2, 3, 4, shown as Fig. 11. Thus the following equation can be derived:

$$C(V_{c2a\max} - V_{c2a\min}) = I_o(1-d)T_s \quad (25)$$

3) Output voltage averaging:

Due to the symmetrical configuration, V_{c2b} possesses the same voltage ripple as V_{c1a} with 180 degree interleaved. Therefore, the output voltage can be approximated as following:

$$V_{out} = V_{c2a\min} + V_{c2a\max} + V_{in} \quad (26)$$

According to equation (20) and (23)~(26), the voltage gain is derived:

$$\frac{V_{out}}{V_{in} - V_d} = \frac{3CR_L(1 - e^{-\frac{2dT_s}{RC}})}{-(dT_s - 3T_s + RC + R_L C)e^{-\frac{2dT_s}{RC}} + 2T_s e^{-\frac{2dT_s}{RC}} + RC + R_L C - dT_s + 3T_s} \quad (27)$$

Where $R=R_1=R_2=r+2R_{on}$.

Meanwhile, the following useful boundaries of flying capacitors are derived:

$$V_{c1a\max} = \frac{-C(-1+a)(R+R_L)(V_d - V_{in}) + ((1+d+2b-3a+da)V_d - (d+b-3a+da)V_{in})T_s}{C(-1+a)(R+R_L) - (-3+d-2b-3a+da)T_s} \quad (28)$$

$$V_{c1a\min} = \frac{-C(-1+a)(R+R_L)(V_d - V_{in}) + ((-3+d+2b+a+da)V_d - (-3+b+d+da)V_{in})T_s}{C(-1+a)(R+R_L) - (-3+d-2b-3a+da)T_s} \quad (29)$$

$$V_{c2a\min} = \frac{-C(-1+a)(R_L V_d + RV_{in}/2 - R_L V_{in}) + (2(1-d)(a-1)V_d - (d+b+3a-2ad)V_{in})T_s}{C(-1+a)(R+R_L) - (-3+d-2b-3a+da)T_s} \quad (30)$$

where $a = e^{\frac{2dT_s}{RC}}$, $b = e^{\frac{dT_s}{RC}}$.

The voltage conversion ratio of equation (27) is plotted in 3-D dimensions as function of duty cycle and frequency, shown in Fig. 13.The circuit parameters are set as Table III.

TABLE III

CIRCUIT PARAMETERS OF 1KW 3X TBSC

Circuit parameters	Value
R_L	80 Ω
V_{in}	100V
r	10m Ω
R_{on}	70m Ω
V_d	0.78V
C	100uF

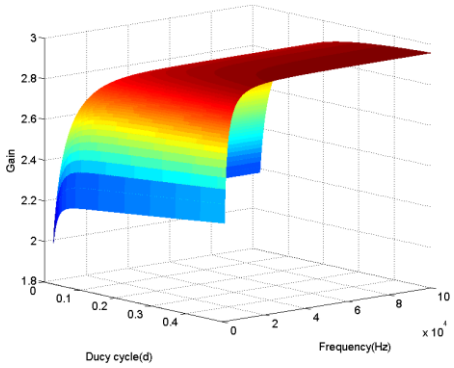

Fig. 13. 3X TBSC voltage gain as function of frequency and duty cycle.

C. Estimation of peak current within charging loop(Ipc) and discharging loop(Ipd)

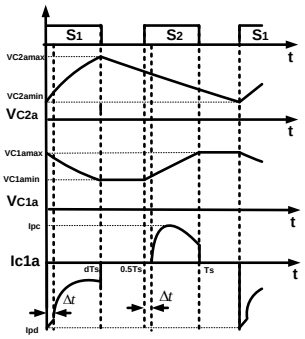

Fig. 14. Transient voltages of capacitor C_{1a}, C_{2a} and transient current of C_{1a}.

Due to coupling loop effect, to derive the expression of current spike is difficult based on normal calculation using precise differential equations within the circuit. Moreover, when switch S_1 is turned on as shown in Fig. 12(b), there is a slight delay of Δt between the conduction of D_{2a} and D_{1b}. The reason is the voltage difference between two flying capacitors C_{1a} and C_{2a} is larger than that of V_{in} and C_{1b}, which causes a rush current in loop 2, leading to the voltage drop on R_{on} high enough to block D_{1b}. When the rush current deceases, voltage drop on R_{on} decreases gradually and D_{1b} starts to conduct. Therefore, the charging current of C_{1b} exhibits a soft rising edge. Similarly, the charging current of C_{1a} has soft rising edge. Therefore, the input current is expected to have soft rising edge with the minimal current set by load current.

The two coupled loops in Fig. 12(b) are defined as one charging loop where C_{1b} is charged and one discharging loop where C_{1a} is discharged. The current waveforms of two coupled loops can be described by the positive part and negative part of current I_{c1a} in Fig. 14 for the sake of symmetry. In the discharging loop, the peak current can be estimated by equation

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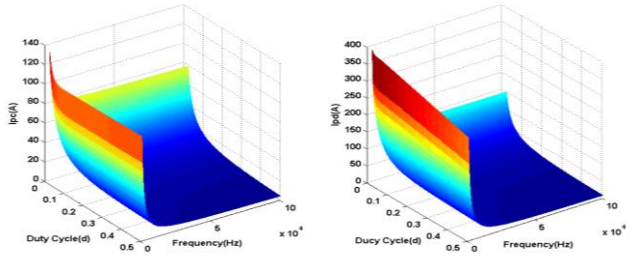
(31), since this peak current occurs before its coupled loop starts conducting:

$$I_{pd} = \frac{V_{c1a\max} - V_{c2a\min} - V_d}{R_{on} + r} \tag{31}$$

For the charging loop, which can be presented as loop 1 in Fig. 12(a), the peak current occurs when both loops are conducted. Therefore, the equivalent loop resistance is used for peak current estimation:

$$I_{pc} = \frac{V_{in} - V_{c1a\min} - V_d}{R} \tag{32}$$

In order to examine the duty cycle and frequency effect on peak currents of charging and discharging loops, equations (31),(32) are plotted as function of duty cycle and frequency in Fig. 15. The other circuit parameters are adopted as Table III except 160 Ω R_L is used here. According to the figure, sufficient large switching frequency is preferred to suppress peak current stress both in charging and discharging loops.



(a) (b)

Fig. 15. Peak current at charging and discharging loops as function of frequency and duty cycle. (a) Charging loop Ipc (b)Discharging loop Ipd

IV. SMALL SIGNAL MODEL OF 3X TBSC CONVERTER

Although the voltage gain shows dependency on both switching frequency and duty cycle, the frequency regulation is still unrealistic due to large current stress when the frequency is low. In higher frequency range, the duty cycle regulation capability is more prominent than frequency regulation, according to Fig. 13. Therefore the duty cycle regulation is adopted for the closed loop design in this paper with a sufficient high switching frequency.

The averaging state space equations of a 3X TBSC converter can be written as:

$$\begin{aligned} \dot{x} &= A_{av}x + B_{av}u \\ x &= [v_{c1a}, v_{c2a}, v_{c1b,}, v_{c2b}]^T \\ u &= v_{in} \end{aligned} \tag{33}$$

Where:

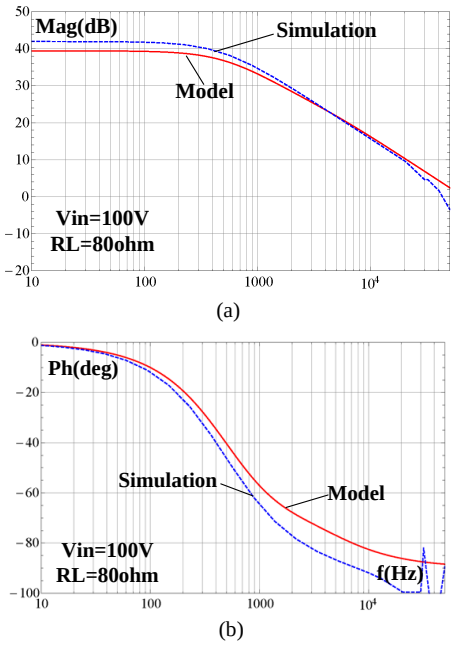
$$A_{av} = \begin{bmatrix} -\frac{2d}{C(r+2R_{on})} & \frac{d}{C(r+2R_{on})} & 0 & 0 \\ \frac{d}{C(r+2R_{on})} & \frac{-dR_L - r - 2R_{on}}{C(r+2R_{on})} & 0 & 0 \\ 0 & 0 & \frac{-2d}{C(r+2R_{on})} & \frac{d}{C(r+2R_{on})} \\ 0 & -\frac{1}{CR_L} & \frac{d}{C(r+2R_{on})} & \frac{-r - dR_L - 2R_{on}}{R_L C(r+2R_{on})} \end{bmatrix}$$

$$B_{av} = \begin{bmatrix} \frac{d}{C(r+2R_{on})} \\ -\frac{1}{CR_L} \\ \frac{d}{C(r+2R_{on})} \\ -\frac{1}{CR_L} \end{bmatrix}$$

By using standard perturbation, the small signal model can be derived. The final analytical expression is not presented due to its tedious expression. However, the numerical transfer functions under V_{in}=100V and R_L=80 Ω is derived as:

$$G(s) = \frac{416378\times(1.18332\times10^{12} + 4.9333910^{8}s + 41975.3s^2 + s^3)}{(5.26285\times10^{15} + 3.67329\times10^{12}s + 7.85742\times10^{8}s^2 + 50620.4s^3 + s^4)} \tag{34}$$

It is compared with simulation result derived from PSIM in Fig. 16. The duty cycle is fixed at 0.17 and other parameters are given as default in Table III. The deviation is expected with regarding to loop decoupling approximation during small signal model derivation process.



(a)

(b)

Fig. 16. Comparison of small signal characteristics between model(solid, red) and psim simulation(dashed, blue) (a)Magnitude (b) Phase

It can be seen the small signal model of 3X TBSC is close to a first order system which can achieve large range stability. Due to constrain of switching frequency in high power condition, a simple PI controller is needed to restrict system bandwidth and control steady state error. The PI parameters are selected using the Matlab sisotool by setting the bandwidth at 1kHz and placing the zero at low frequency pole of open loop system, therefore we get:

$$C_c = 0.005+100/s \tag{35}$$

After compensation, the loop gain bandwidth is shrined from around 50 kHz to 1 kHz, as shown in Fig. 17. In circuit prototype, 40 kHz switching frequency is adopted which is forty times of circuit bandwidth.

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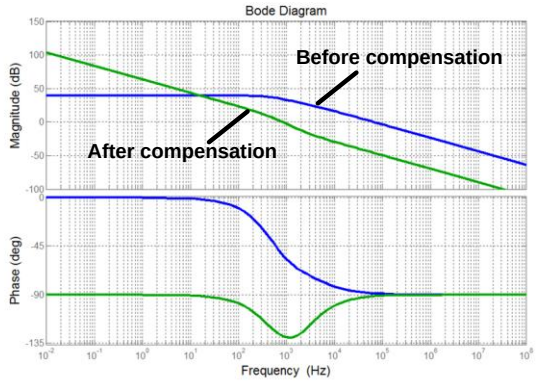


Fig. 17. Loop gain bode plot comparison before and after compensation

V. SIMULATION AND EXPERIMENTAL VARIFICATION

A. *Simulation verification of CT and current stress model*

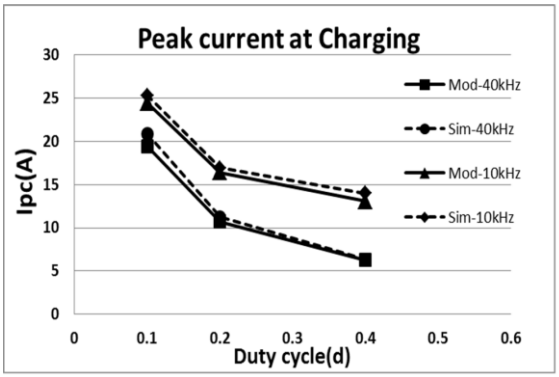
In order to verify the accuracy of CT method and peak current stress model, the simulation results are compared with the model calculation, with various operation conditions of switching frequency and duty cycle. The results are presented in Table IV and Fig. 18. The load is set as 160 Ω and other parameters are chosen as default in Table III.

According to Table IV, The CT modeling method is confirmed by precisely agreements between simulation result and model prediction for boundary voltages of C_{1a} and C_{2a}. Based on Fig. 18, the peak current model is verified which can provide more guidance for engineers in semiconductor components selection.

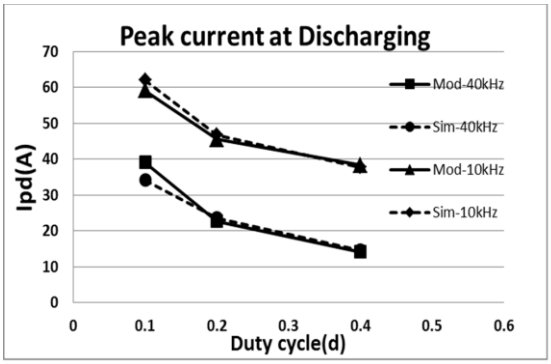
B. *Experimental Results*

A 1kW 3X TBSC converter prototype is built as shown in Fig. 19.The peak current stress within charging and discharging loops can be indicated by measuring the current of capacitor C_{1a}. The input voltage is fixed at 100V and load at 160 Ω . The tested results are shown in Fig. 20 by varying switching frequency and duty cycle. Frequency range below 5 kHz switching frequency is not tested due to the current stress limitation of circuit components.

In real circuit, current spike is very sensitive to PCB parasitic



(a)



(b)

Fig. 18. Comparison of peak current model with simulation(a) Peak current comparison at charging phase (b)Peak current comparison at discharging phase

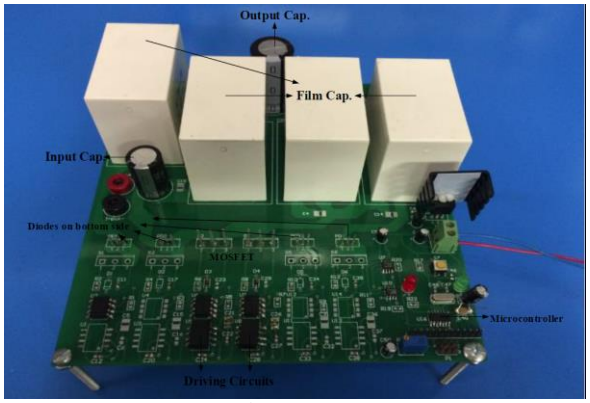


Fig. 19. Experimental prototype of 1kW 3X TBSC

TABLE IV

VERIFICATION OF CT MODEL

f(Hz)	d	**Vc1amax(V) (model)**	Vc1amax**(V)** (sim)	error	**Vc1amin(V) (model)**	Vc1amin**(V)** (sim)	error	**Vc2amin(V) (model)**	Vc2amin**(V)** (sim)	error
40k	0.1	**96.7552**	96.79	-0.036%	**96.3082**	96.34	-0.033%	**92.8449**	92.81	0.038%
40k	0.2	**98.0695**	98.09	-0.021%	**97.6143**	97.64	-0.026%	**95.4692**	95.4	0.073%
40k	0.4	**98.7354**	98.76	-0.025%	**98.2762**	98.3	-0.024%	**96.8199**	96.79	0.031%
10k	0.1	**97.3388**	97.51	-0.176%	**95.556**	95.73	-0.182%	**91.8252**	91.71	0.126%
10k	0.2	**98.5718**	98.68	-0.110%	**96.7608**	96.87	-0.113%	**94.1528**	94.12	0.035%
10k	0.4	**99.0839**	99.09	-0.006%	**97.2616**	97.26	0.002%	**95.2374**	95.25	-0.013%
1k	0.1	**99.20**	99.16	0.040%	**83.5066**	83.4	0.128%	**68.4849**	68.4	0.124%
1k	0.2	**99.22**	99.16	0.061%	**83.4411**	83.24	0.242%	**69.9196**	69.7	0.315%

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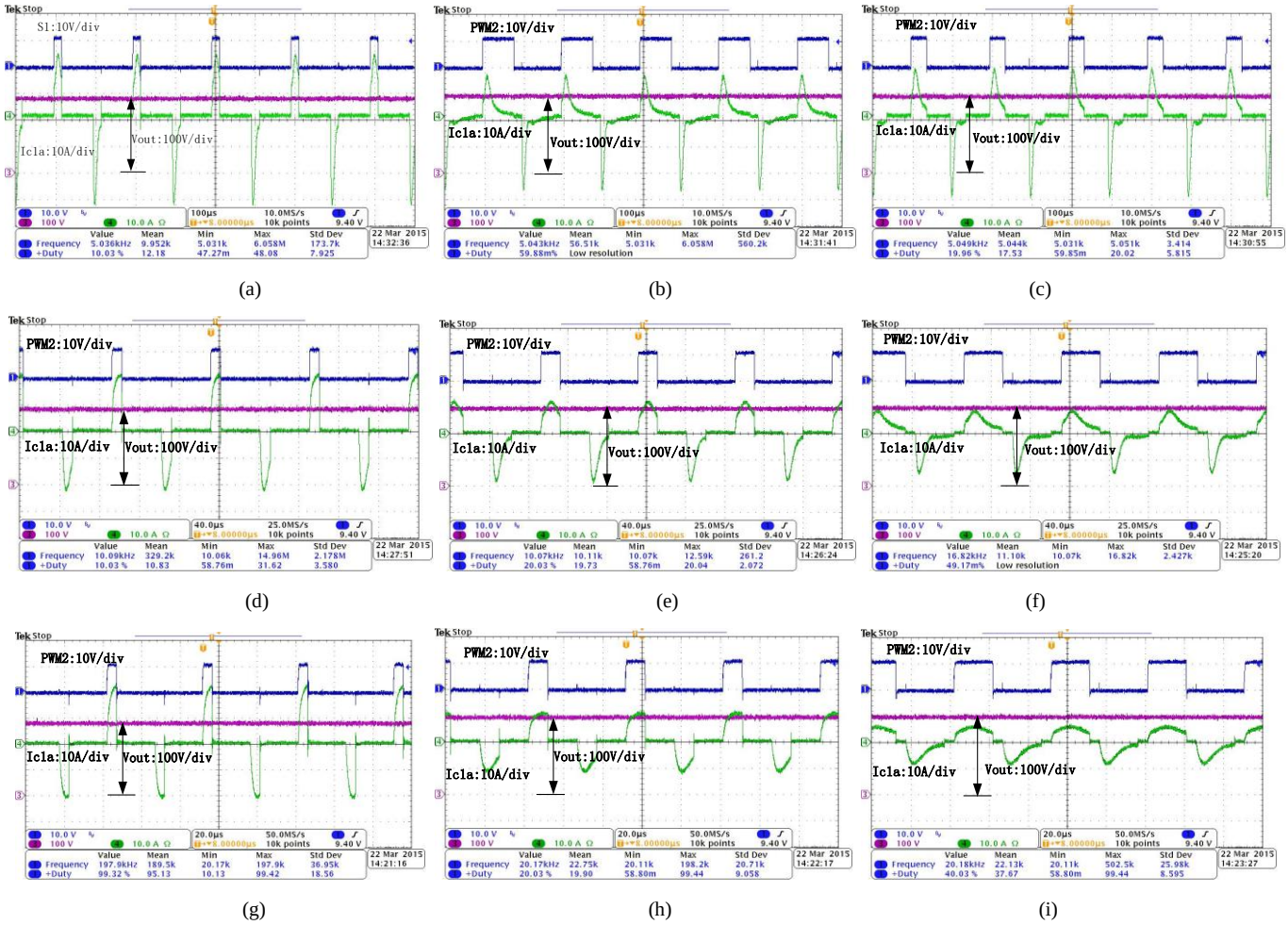

Fig. 20. Waveforms of PWM, V_{out}, I_{c1a} under R_L=160 Ω (a)f=5k, d=0.1 (b)f=5k, d=0.2 (c)f=5k, d=0.4(d)f=10k, d=0.1 (e)f=10k, d=0.2 (f)f=10k, d=0.4 (h)f=20k, d=0.1 (i)f=20k, d=0.2 (j)f=20k, d=0.4

parameters which prevents it from matching the model and simulation results closely. However, the current waveforms agree well with simulation. Frequency effect on peak current stress is also demonstrated.

C. *Input current under rated power*

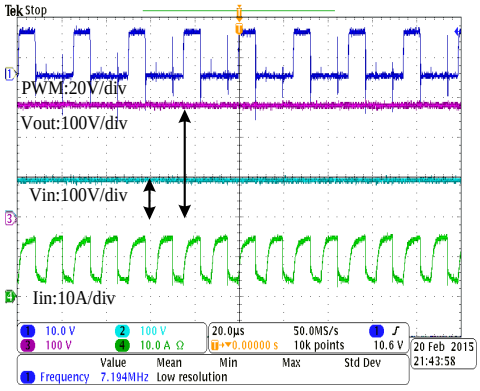

Fig. 21. Experimental waveforms of PWM, V_{out}, V_{in} and I_{in}

According to discussion in section IV-C, input current with soft rising edge should be expected. The experimental results are given as Fig. 21 under rated power condition with switching frequency of 40 kHz. The waveforms of driving signal, input voltage, output voltage and input current are presented and soft rising edge for input current is observed.

D. *Close loop operation under load step condition*

With the designed PI controller, the converter is operated under closed loop and tested with load step. The output power is switched between 1000W and 500W while the output voltage can be maintained constant after small disturbance. The testing results are shown in Fig. 22. It can be seen the input current exhibit limited peak current under different load conditions as well as step transient.

VI. CONCLUSION

A Charge-Balance Transient-Calculation modeling method for SCC is explored and investigated in this paper for steady state analysis of high power SCC. Its accuracy is confirmed by comparison with traditional modeling methods. It provides overall circuit parameters impacts on conversion ratio, which is essential for converter optimization.

Based on the CT model, a peak current stress estimation method is derived for high power SCC design with consideration of incorporating moderate regulation. The peak

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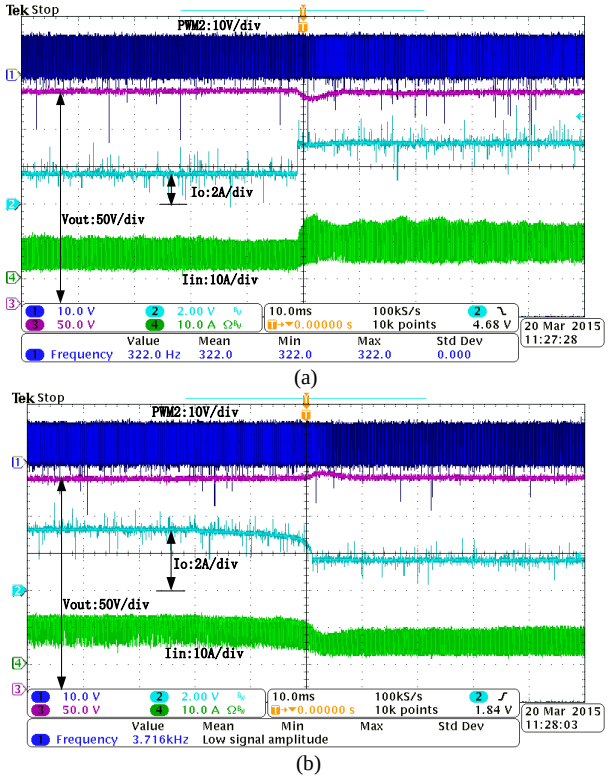

Fig. 22. Load step with V_{in}=100V, V_{out}=280V(a)Load step from 160 Ω to 80 Ω (b) Load step from 80 Ω to 160 Ω

current stress model captures the duty cycle and frequency effect on circuit stress and provides guidance of regulation range selection under fixed circuit parameters. A 1kW 3X TBSC topology is analyzed using CT modeling method and peak current stress estimation. It's soft rising input current property is also exhibited with the aid of coupled SC loops. The small signal model of 3X TBSC is derived and closed loop operation is achieved with the proper choice of regulation range. The simulation and experimental results confirm the theoretical analysis and demonstrate the feasibility of moderate regulation capability design for high power switched capacitor converters.

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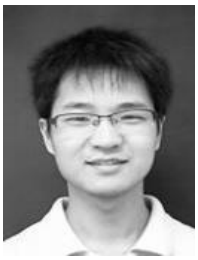

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