EFFECT OF GATE PULSE VARIATION ON THE PERFORMANCE OF FIFTEEN-LEVEL CASCADED H-BRIDGE VOLTAGE SOURCE INVERTER

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ABSTRACT

This paper proposes a fifteen level H- Bridge cascaded multilevel inverter with fundamental frequency switching for low power applications such as solar powered power supplies, battery powered standby power supplies. The effect of the variation of gate pulse on the performance of the inverter for different conditions of gate pulse variation is studied and simulation results are presented. Experimental implementation of gate pulse generation on a low cost FPGA is presented. The results presented in this paper are useful in designing the inverter, determining the control range of the inverter for the reliable and stable closed loop and fault tolerant operation of the inverter.

Index Terms— Cascade H- Bridge inverter, voltage source inverter, *THD*.

1. INTRODUCTION

Cascaded H-bridge multilevel inverters are widely used in high power applications [1-5]. This inverter topology has some useful features such as high reliability [5], modularity [3], fault tolerant features [4], ability to synthesize the sinusoidal waveforms with fundamental switching frequency at high levels [3-5]. These characteristics are also useful in low and medium power (few hundreds of watts to 500Kw) applications such as photovoltaic power supplies and uninterrupted power supplies (UPS). The advantage of the proposed topology over conventional inverter topology is that the proposed topology results in efficient energy conversion and reliable operation. Also this topology works satisfactorily even under faulty conditions. The inverter devices are switched at fundamental frequency hence the switching losses are reduced at the same time sinusoidal output voltage waveforms are synthesized [2-6].

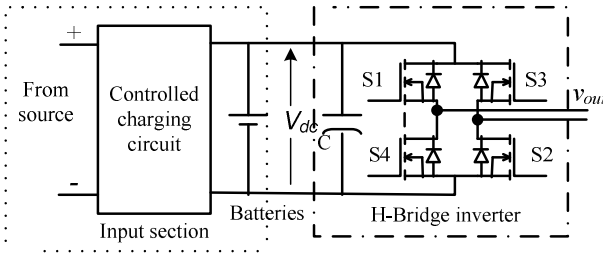

Fig. 1. Power circuit schematic of one H-Bridge cell.

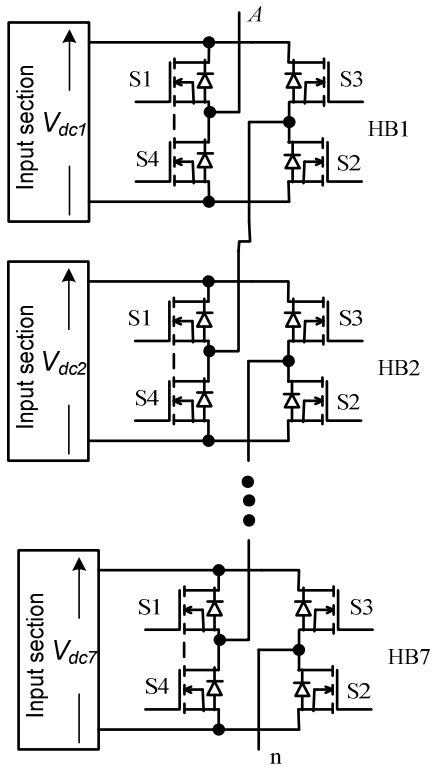

Fig. 2. Power circuit schematic of cascaded fifteen-level H-Bridge.

The modular structure results in reliable operation and satisfactory performance under faulty conditions [5]. Also the desired voltages can be synthesized using low voltage MOSFETs which results in reduced conduction loss [3].

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It is shown that with fundamental switching frequency, the THD is low if the number of levels is higher than 11 [3]. Hence a fifteen level inverter topology is considered in the present work. The fifteen-level inverter given in [3] has some useful features but its performance is studied only in open loop. In photovoltaic power supplies and UPS systems, output voltage regulation is essential. Output voltage regulation can be achieved by closed loop operation of the inverter. The output voltage has to be maintained constant against the variation of source voltage and load. Closed loop operation is also required for the active and reactive power flow control when the above systems are integrated with the power grid. In closed loop operation the operating point or gate pulse width will vary around the steady state operating point. Depending on the system requirements, the inverter will operate at new operating point. This means the gate pulse width will change with new operating point.

The main contribution of this paper is that it presents the effect of gate pulse variation on inverter output voltage. Different operating conditions that result in gate pulse variation are simulated and results are tabulated. These results form the basis for the design of controller for satisfactory operation of the inverter over the control range. Also this information is useful for the downgraded operation of the inverter under fault conditions. The system is simulated in MATLAB/SIMULINK software. A simple FPGA implementation of the above system and gate pulse generation is presented.

2. Fifteen Level Cascaded H-Bridge Inverter

The power circuit of the one H-Bridge cell of the fifteen-level H- bridge cascaded inverter is shown in fig.1. Only a brief description is given in this section, since the present work is extension of work presented in [3] and the details are available in [3]. Each H-Bridge cell consists of an H-Bridge inverter and input section. The source may be photovoltaic cells or rectified output from a step down transformer or any other isolated dc supply. The inverter has seven such identical bridges, HB1 to HB7 which are cascaded together as shown in fig.2, to get 15-level inverter topology [3]. In each bridge when devices S1 and S4 are on, output voltage is V_{dc} volts (state 1), for state 0 either S1 and S3 or S2 and S4 are on and the output voltage is 0 volts. When devices S3 and S2 are on, the output voltage is $-V_{dc}$ volts and it is said to be in state -1. The application is for 220V, 50Hz single phase system. The voltage across each bridge is about 48 volts that is $V_{dc}= V_{dc1} = V_{dc2}= V_{dc3}= V_{dc4}= V_{dc5} = V_{dc6}= V_{dc7}$=48 volts. So the low voltage MOSFETs (with voltage rating 0f 100V) are used as switches. The low voltage MOSFET has low R_{DSon} which reduces the conduction loss compared to IGBTs and other power semiconductor devices [3,4]. Since the fundamental switching frequency is used, the switching losses are very low [3,5,7,10]. Hence this configuration has dual advantages that it has low switching loss as well as low conduction loss which is a desirable feature especially in battery powered or solar powered power supplies.

3. Fundamental Frequency Switching of Inverter

The output voltage of the fifteen-level inverter with fundamental frequency switching is as shown in fig.3. The voltage is a stepped sine wave. The deviation from the sine wave gives a measure of THD content of the waveform. The staircase waveform given in fig. 3 can be represented interims of Fourier coefficients as follows [1,4,6]

$$V(\omega t) = \sum_{n=1,3,5...}^{\infty} \frac{4V_{DC}}{n\pi}[\cos(n\theta_1)+\cos(n\theta_2)+... + \cos(n\theta_m)]*\sin(\omega t), \quad (1)$$

where m is the number of H-Bridge inverters; m=1,2…7. θ= Firing Angle and $\theta_1 < \theta_2 < ... < \theta_m$.

There are several approaches for the determination of gate pulses. The simple one is sine-step comparison approach,

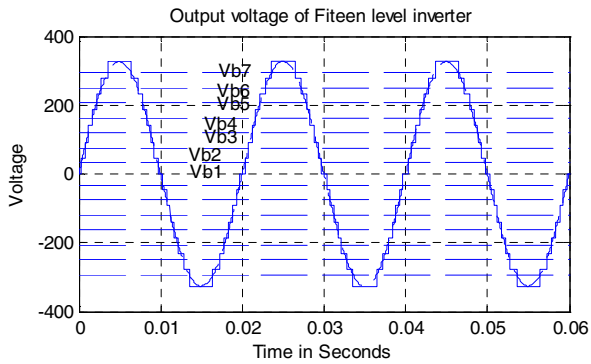

Fig 3. Voltage waveform of fifteen-level inverter

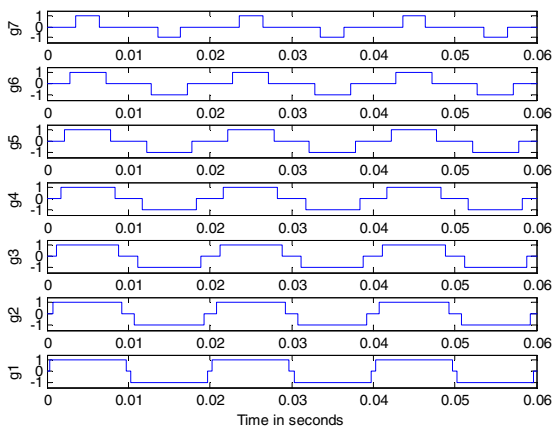

Fig . 4. Switching logic for the 7 H-Bridges

in which the gating instant is determined by intersecting the dc step voltage with the desired sine wave [3]. This approach results in a symmetrical staircase waveform as shown in fig.3. In fig.3, horizontal lines represent the dc voltages, Vb1=V_{dc}, Vb2=2 V_{dc}, Vb3=3 V_{dc}, Vb4=4 V_{dc}, Vb5=5 V_{dc}, Vb6=6 V_{dc} and Vb7=7 V_{dc} for balanced sources. The other switching strategies are, to use different angles, different voltage levels, etc [6,7,10]. In this approach the switching angles are decided to achieve certain optimal criteria, most widely used optimal criteria

is minimizing the THD of the output voltage or dc bus balancing approach [6,7,10]. However these methods are not suitable for closed loop operation, required offline computation and highly computational intensive compared to the sine-step comparison method. Since the present work focuses on closed loop operation of the inverter, sine-step comparison method is used. Fig.4 shows the switching logic for equal dc voltages. In fig. 4, logic 1 indicates that the switches S1 and S2 of the given cell are on. For logic -1, switches S3 and S4 of the given cell are on. Switches S1 and S3 are on during logic 0 state, which lay between logic 1 and logic -1 state. Similarly switches S2 and S4 are on during logic 0 state, which lay between logic -1 and logic 1 state. This ensures that all the four switches in a cell are uniformly loaded and have equal duty cycle. Owing to the large number of steps, the output waveform has very low the *THD*. For the waveform given in fig.3, the *THD* is 0.0565.

4. Gate Pulse Variation: Simulation Results

In order to have a satisfactory performance of the inverter in the control region, it is necessary to study the effect of switching instant variation on the inverter performance.

4.1. Case (i) : Equal variation of gate pulses:

Switching instants of all the H-Bridges are varied equally i.e. $\theta_{1new} = \theta_1 + \Delta\theta; \theta_{2new} = \theta_2 + \Delta\theta$ and so on.

This situation arises when all the dc sources are balanced and load varies. In this case the switching angle is increased or reduced in equal interval in the range of 1% to 10% and its effect on output *THD* is studied. The actual *THD* v/s $\Delta\theta$ is plotted in fig 5. As expected the *THD* increases as we move away from the set point. The distortion is higher, if the change of gate pulse is large.

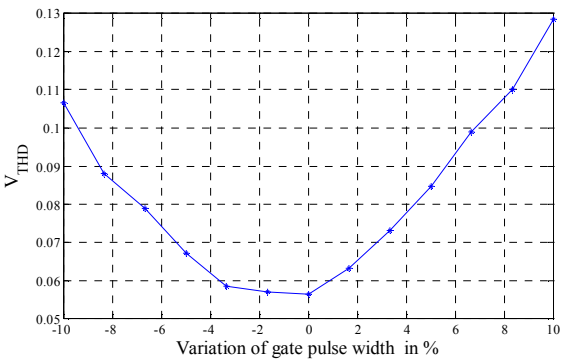

Fig 5. Actual V_{THD} v/s $\Delta\theta$

4.2. Case (ii) Unequal variation of the switching angles:

Unequal variation is required when the dc sources are unbalanced or on or more H-bridge is faulty. The dc source imbalance may come due to partial covering of the solar panels due to cloud or shadow or sand collection or birds or imbalance in the battery due to battery characteristics, battery life etc. Several scenarios can take place under this condition.

Scenario 1: Gate pulse width of one of the H-bridge (HB1) is unaltered and all other H-bridge switching angles are altered by equal amount. The simulation is carried out for +/- 1.5% and +/-10% variation of pulse width for all the six bridges except the HB1. The results are tabulated in Table 1.

Table 1. Gate pulse width of all except HB1 are varied.

Gate pulse variation	*+1.5%*	-1.5%	+10%	-10%
V_{THD} *(Actual)*	.075	0.069	.1321	0.1132

Scenario 2: There may be a case where about 50% of the H-bridges will have normal or higher dc bus voltage and these will have increased gate pulse width. Other 50% H-bridges will have reduced dc bus voltage and their gate pulse width will reduce. The simulation is carried out for +/-3% and +/-5% variation of gate pulse width. The results are tabulated in Table 2.

Table 2. Four H-Bridge gate pulse width are increased and that of other 3 are reduced.

Gate pulse variation	*+3%*	-3%	+5%	-5%
V_{THD} *(Actual)*	0.0876	0.0667	0.0865	0.0742

Scenerio 3: Gate pulse width of the H-Bridges is varied among the bridges randomly, that is in some it is increased, for others it is reduced. The output *THD* for +10% and -10% gate pulse variation in one of the bridges in tabulated in Table 3 and Table 4 respective.

Table 3. The gate pulse width is changed randomly by +10%

Gate pulse variation	*V2*	V3	V4	V5	V6	V7
V_{THD} *(Actual)*	0.0962	0.1041	0.093	0.0921	0.0908	0.0925

Table 4. The gate pulse width is changed randomly by-10%

Gate pulse variation	*V2*	V3	V4	V5	V6	V7
V_{THD} *(Actual)*	0.0734	0.0757	0.784	0.0808	0.0849	0.0897

5. Experimental Implementation

Field Programmable Gate Arrays (FPGA) is becoming alternative solution for the realization of digital control systems. The FPGA based controllers offer advantages such as high speed computation, complex functionality, real time processing capabilities, low power consumption and re-configurability. In this paper the digital controller

for fifteen-level inverter is implemented using Altera based cyclone family EP1C12Q240C8 FPGA which runs at 28MHz clock frequency. The Register Transfer Level (RTL) implementation for the controller is written in very high speed integrated circuit hardware description language (VHDL), synthesized using an Altera based Quartus II 9.0 as a foundation tool. The FPGA simulation

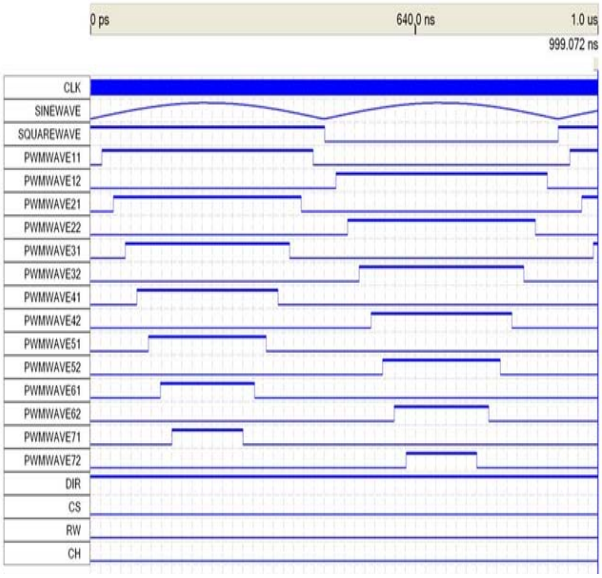

Fig.6 Pulses for fifteen-level synthesized in Altera Quartus II 9.0.

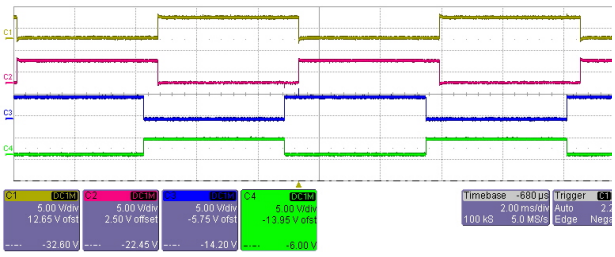

Fig.7 Gate pulses for one of the H-Bridge. C1 is for S1, C2 for S4, C3 for S3 and C4 for S2. (Scale: y-axis : 5v/div, x-axis : 5msec/div

and synthesized results are shown in fig.6. The educational version has memory limitation and in order to overcome this problem, the simulation is carried out in compressed time scale for 1000ns with step size of 100ps as shown in fig.6. This is carried out only to test the program and validate the circuit. However the actual pulses are in real-time to match the load requirements. The output bit file is targeted to the board to generate gate pulses. The gate pulses for individual MOSFETs of H-Bridge are generated by logically splitting the gate pulses generated for the H-Bridge cell. The FPGA board gives out pulses at 3.3V logic levels. This is converted to 5V logic level in interface card to get higher noise immunity. Finally the pulses are converted to +/- 15V CMOS logic level in the MOSFET gate drive circuit. The typical gate pulses of all the four MOSFETs of H-Bridge 1, at the output of the FPGA controller are shown in fig 7. All the four switches have equal duty cycle.

6. CONCLUSIONS

A fifteen level cascaded H-bridge inverter for low power applications is considered. Effect of gate pulse variation on the output voltage is studied for different operating scenarios. The results on *THD* variation against the gate pulse variation are presented. These results are useful in defining the close loop operation range of the power supplies. Also these results will be useful in determining the operation of the inverter under faulty conditions. Generation of gate pulses on a FPGA based digital controllers is presented.

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