A Zero-Voltage-Switching DC–DC Converter With High Voltage Gain

Hyun-Lark Do

***Abstract*—A zero-voltage-switching (ZVS) dc–dc converter with high voltage gain is proposed. It consists of a ZVS boost converter stage and a ZVS half-bridge converter stage and two stages are merged into a single stage. The ZVS boost converter stage provides a continuous input current and ZVS operation of the power switches. The ZVS half-bridge converter stage provides a high voltage gain. The principle of operation and system analysis are presented. Theoretical analysis and performance of the proposed converter were verified on a 100 W experimental prototype operating at 108 kHz switching frequency.**

***Index Terms*—Boost converter, coupled inductor, high voltage gain, reverse recovery, zero-voltage switching (ZVS).**

I. Introduction

DC–DC converters with high voltage gain are required in many industrial applications such as the front-end stage for the renewable and green energy sources including the solar arrays and the fuel cells, the power systems based on battery sources and super capacitors [1]–[6].

IN dc–dc converters with high voltage gain, there are several requirements such as high voltage gain [2], [3], [5], [6], low reverse-recovery loss [7], [8], soft-switching characteristic [16], low-voltage stress across the switches, electrical isolation, continuous input current, and high efficiency. In order to meet these requirements, various topologies are introduced. In order to extend the voltage gain, the boost converters with coupled inductors are proposed in [9] and [10]. The voltage gain is extended but continuous input current characteristic is lost and the efficiency is degraded due to hard switching of power switches. In [11], a step-up converter based on a charge pump and coupled inductor is suggested. Its voltage gain is around 10 but its efficiency is not high enough due to the switching loss. In [12], a high-step-up converter with coupled inductors is suggested to provide high voltage gain and a continuous input current. However, its operating frequency is limited due to the hard switching of the switches. The converters suggested in [13]–[15] have a similar drawback. Their switching frequencies are limited due to the hard-switching operation. In order to increase the efficiency and power density, soft-switching technique is required in dc–dc converters. In [16]–[24], various soft-switching techniques are suggested. Generally, there is a tradeoff between soft-switching characteristic and high voltage gain. It is because an inductor that is related with soft-switching limits the voltage gain.

In order to solve these problems, a zero-voltage-switching (ZVS) dc–dc converter with high voltage gain is proposed. As shown in Fig. 1, it consists of a ZVS boost converter stage to make the input current continuous and provide ZVS functions and a ZVS half-bridge converter stage to provide high voltage gain. Since single power processing stage can be a more efficient and cost-effective solution, both stages are merged and share power switches to increase the system efficiency and simplify the structure. Since both stages have the ZVS function, ZVS operation of the power switches can be obtained with wider load variation. Moreover, due to the ZVS function of the boost converter stage, the design of the half-bridge converter stage can be focused on high voltage gain. Therefore, high voltage gain is easily obtained. ZVS operation of the power switches reduces the switching loss during the switching transition and improves the overall efficiency. The theoretical analysis is verified by a 100 W experimental prototype with 24–393 V conversion.

II. Analysis of the Proposed Converter

The equivalent circuit of the proposed converter is shown in Fig. 2. The ZVS boost converter stage consists of a coupled inductor L_c, the lower switch Q_1, the upper switch Q_2, the auxiliary diode D_a, and the dc-link capacitor $C_{\rm dc}$. The diodes D_{Q1} and D_{Q2} represent the intrinsic body diodes of Q_1 and Q_2. The capacitors C_{Q1} and C_{Q2} are the parasitic output capacitances of Q_1 and Q_2. The coupled inductor L_c is modeled as the magnetizing inductance L_{m1}, the leakage inductance L_{k1}, and the ideal transformer that has a turn ratio of 1:n_1 ($n_1 = N_{s1}/N_{p1}$). The ZVS half-bridge converter stage consists of a transformer *T*, the switches Q_1 and Q_2, the output diodes D_{o1} and D_{o2}, the dc-blocking capacitors C_{B1} and C_{B2}, and the output capacitor C_o. The transformer *T* is modeled as the magnetizing inductance L_{m2}, the leakage inductance L_{k2}, and the ideal transformer that has a turn ratio of 1:n_2 ($n_2 = N_{s2}/N_{p2}$). The theoretical waveforms of the proposed converter are shown in Fig. 3. The switches Q_1 and Q_2 are operated asymmetrically and the duty ratio *D* is based on the switch Q_1. The operation of the proposed converter in one switching period T_s can be divided into seven as shown in Fig. 4. Just before Mode 1, the upper switch Q_2, the auxiliary diode D_a, and the output diode D_{o1} are conducting. The magnetizing current i_{m1} of L_c arrives at its minimum value I_{m12} and the auxiliary diode current $i_{\rm Da}$ arrives at its maximum value $I_{\rm Da}$. The current i_L has its maximum value I_{L1}.

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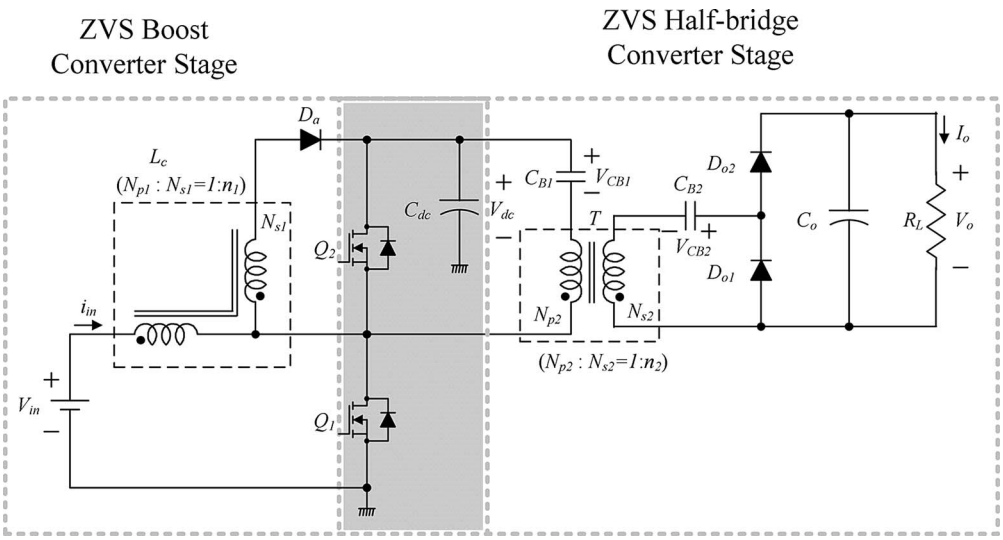


Fig. 1 Proposed soft-switching dc–dc converter with high voltage gain.

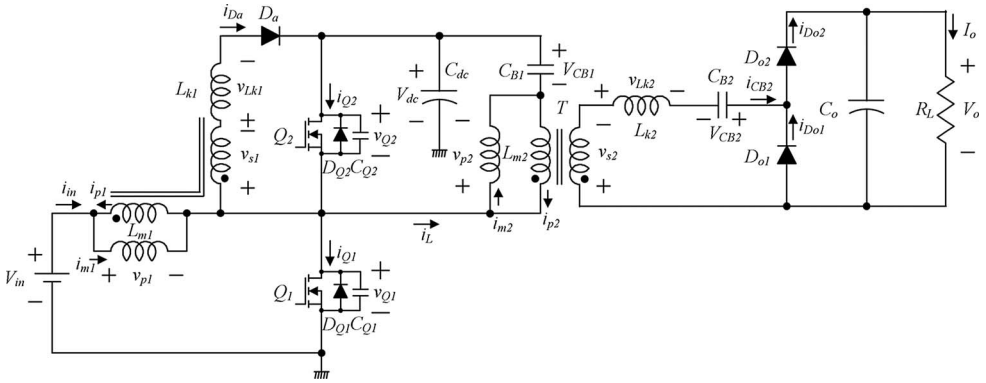


Fig. 2 Equivalent circuit of the proposed soft-switching dc–dc converter.

Mode 1 [t_0, t_1]: At t_0, the upper switch Q_2 is turned OFF. Then, the capacitor C_{Q2} starts to be charged and the voltage v_{Q2} across Q_2 increases toward $V_{\rm dc}$. Simultaneously, the capacitor C_{Q1} is discharged and the voltage v_{Q1} across Q_1 decreases toward zero. With an assumption that the output capacitances C_{Q1} and C_{Q2} of the switches are very small and all the inductor currents are not changed, the transition time interval T_{t1} can be considered as follows:

$$T_{t1} = t_1 - t_0 = \frac{(C_{Q1} + C_{Q2})V_{dc}}{I_{L1} + (n_1 + 1)\, I_{\rm Da} - I_{m12}}. \tag{1}$$

Mode 2 [t_1, t_2]: At t_1, the voltage v_{Q1} across the lower switch Q_1 becomes zero and the body diode D_{Q1} is turned ON. Then, the gate signal for Q_1 is applied. Since the current has already flown through the body diode D_{Q1} and the voltage v_{Q1} is maintained as zero before the switch Q_1 is turned ON, the zero-voltage turn-ON of Q_1 is achieved. Since the voltage v_{p1} across the magnetizing inductance L_{m1} is $V_{\rm in}$, the magnetizing current i_{m1} increases linearly from its minimum value I_{m2} as follows:

$$i_{m1}(t) = I_{m12} + \frac{V_{\rm in}}{L_{m1}}\,(t - t_1)\,. \tag{2}$$

Since the voltage $v_{\rm Lk1}$ across the leakage inductance L_{k1} is $-(n_1 V_{\rm in} + V_{\rm dc})$, the auxiliary diode current $i_{\rm Da}$ linearly decreases from its maximum value $I_{\rm Da}$ as follows:

$$i_{\rm Da}(t) = I_{\rm Da} - \frac{n_1 V_{\rm in} + V_{\rm dc}}{L_{k1}}(t - t_1). \tag{3}$$

From (2) and (3), the input current $i_{\rm in}$ is determined as follows:

$$i_{\rm in}(t) = i_{m1}(t) - i_{p1}(t) = i_{m1}(t) - n_1 i_{\rm Da}(t) = I_{m12} - n_1 I_{\rm Da} + \frac{V_{\rm in}}{L_{m1}}\,(t - t_1) + n_1 \cdot \frac{n_1 V_{\rm in} + V_{\rm dc}}{L_{k1}}\,(t - t_1)\,. \tag{4}$$

Since v_{p2} is $-(V_{\rm dc} - V_{\rm CB1})$ and v_{Lk2} is $V_{\rm CB2} + n_2 V_{\rm in}$, the magnetizing current i_{m2} and the diode current i_{Do1} are given by

$$i_{m2}(t) = I_{m21} - \frac{V_{\rm dc} - V_{\rm CB1}}{L_{m2}}\,(t - t_1) \tag{5}$$

$$i_{Do1}(t) = -i_{\rm CB2}(t) = I_{Do1} - \frac{V_{\rm CB2} + n_2 V_{\rm in}}{L_{k2}}\,(t - t_1)\,. \tag{6}$$

In this mode, the primary current i_{p2}, the coupled inductor current i_L, and the switch current i_{Q1} can be obtained from

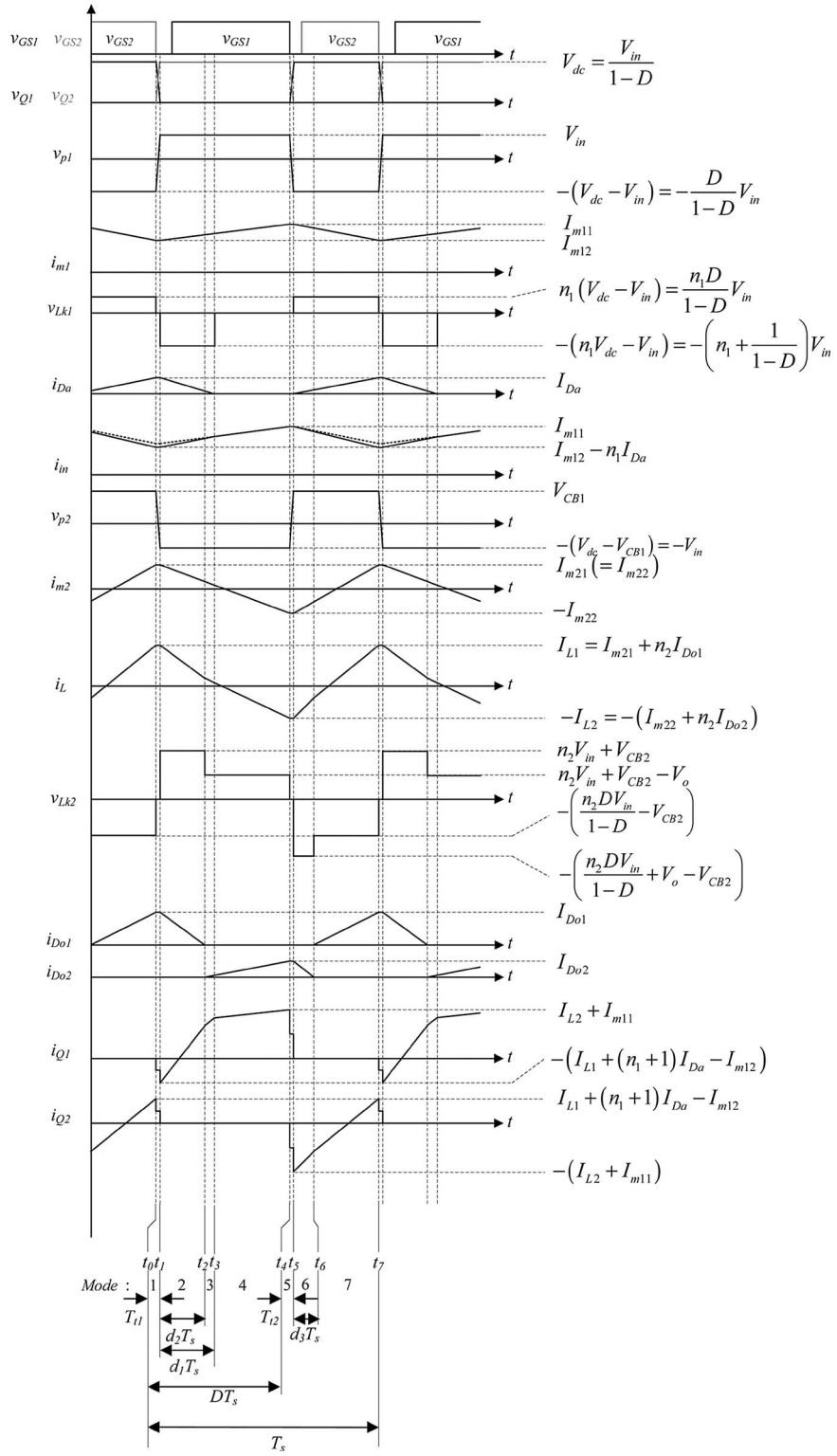


Fig. 3 Theoretical waveforms.

the following relations:

$$i_{p2}(t) = n_2 i_{\mathrm{CB2}}(t) \tag{7}$$

$$i_L(t) = i_{m2}(t) - i_{p2}(t) \tag{8}$$

$$i_{Q1}(t) = i_{\mathrm{in}}(t) - i_{\mathrm{Da}}(t) - i_L(t). \tag{9}$$

Mode 3 [t_2, t_3]: At t_2, the current i_{CB2} changes its direction. The output diode current i_{Do1} decreases to zero and the diode D_{o1} is turned OFF. Then the output diode D_{o2} is turned ON and its current increases linearly. Since the current changing rate of D_{o1} is controlled by the leakage inductance L_{k2} of the transformer *T*, its reverse-recovery problem is alleviated. Since

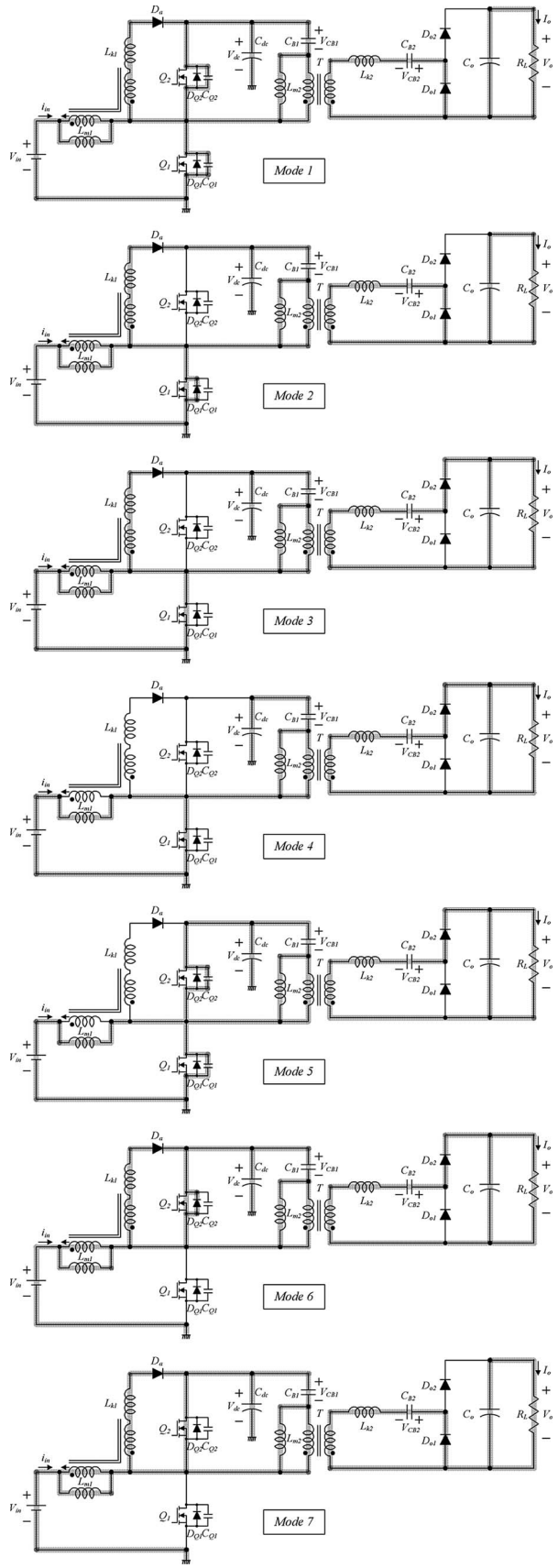


Fig. 4 Operating modes.

v_{p2} is the same as in Mode 2 and $v_{\mathrm{Lk}}2$ is $n_2V_{\mathrm{in}}+V_{\mathrm{CB2}}–V_o$, the current i_{m2} and the diode current i_{Do2} are given by

$$i_{m2}(t) = i_{m2}(t_2) - \frac{V_{\mathrm{in}}}{L_{m2}}(t-t_2) \tag{10}$$

$$i_{Do2}(t) = i_{\mathrm{CB2}}(t) = \frac{V_{\mathrm{CB2}} + n_2V_{\mathrm{in}} - V_o}{L_{k2}}(t-t_2). \tag{11}$$

The currents i_{p2}, i_L, and i_{Q1} can be obtained from the same relations in Mode 2. In this mode, the voltages v_{p1} and v_{Lk} are equal to those in Mode 2. Therefore, the magnetizing current i_{m1}, the auxiliary current i_{Da}, and the input current i_{in} change with the same slopes as in Mode 2.

Mode 4 [t_3, t_4]: At t_3, the auxiliary diode current i_{Da} decreases to zero and the diode D_a is turned OFF. Since the changing rate of the diode current i_{Da} is controlled by the leakage inductance L_{k1} of the coupled inductor L_c, its reverse-recovery problem is alleviated. Since the voltage v_{p1} across the magnetizing inductance L_{m1} is the input voltage V_{in}, the magnetizing current i_{m1} increases linearly with the same slope as in Modes 2 and 3 as follows:

$$i_{m1}(t) = i_{m1}(t_3) + \frac{V_{\mathrm{in}}}{L_{m1}}(t-t_3). \tag{12}$$

Since the auxiliary diode current i_{Da} is zero, the input current i_{in} is equal to the magnetizing current i_{m1}. At the end of this mode, the magnetizing current i_{m1} arrives at its maximum value I_{m11}. Since the voltages v_{p2} and $v_{\mathrm{Lk}2}$ are not changed in this mode, the slopes of the current i_{m2}, i_{CB2}, and i_L are not changed.

Mode 5 [t_4, t_5]: At t_4, the lower switch Q_1 is turned OFF. Then, the capacitor C_{Q1} starts to be charged and the voltage v_{Q1} across Q_1 increases toward V_{dc}. Simultaneously, the capacitor C_{Q2} is discharged and the voltage v_{Q2} across Q_2 decreases toward zero. With the same assumption as in Mode 1, the transition time interval T_{t2} can be determined as follows:

$$T_{t2} = t_5 - t_4 = \frac{(C_{Q1}+C_{Q2})V_{\mathrm{dc}}}{I_{L2}+I_{m11}}. \tag{13}$$

Mode 6 [t_5, t_6]: At t_5, the voltage v_{Q2} across the upper switch Q_2 becomes zero and the body diode D_{Q2} is turned ON. Then, the gate signal is applied to the switch Q_2. Since the current has already flown through the body diode D_{Q2} and the voltage v_{Q2} is maintained as zero before the turn-ON of the switch Q_2, the zero-voltage turn-ON of Q_2 is achieved. Since the voltage v_{p1} across the magnetizing inductance L_{m1} is –(V_{dc}–V_{in}), the magnetizing current i_{m1} decreases linearly from its maximum value I_{m11} as follows:

$$i_{m1}(t) = I_{m11} - \frac{V_{\mathrm{dc}} - V_{\mathrm{in}}}{L_{m1}}(t-t_5). \tag{14}$$

Since the voltage v_{Lk1} across the leakage inductance L_k is n_1(V_{dc}–V_{in}), the auxiliary diode current i_{Da} linearly increases from zero as follows:

$$i_{\mathrm{Da}}(t) = \frac{n_1(V_{\mathrm{dc}} - V_{\mathrm{in}})}{L_{k1}}(t-t_5). \tag{15}$$

From (14) and (15), the input current $i_{\rm in}$ is determined as

$$i_{\rm in}(t) = I_{m11} - \frac{V_{\rm dc} - V_{\rm in}}{L_{m1}}(t - t_5) - \frac{n_1^2 (V_{\rm dc} - V_{\rm in})}{L_{k1}}(t - t_5). \tag{16}$$

Since the voltage v_{p2} is $v_{\rm CB1}$ ($= DV_{\rm in}/(1–D)$) and $v_{\rm Lk2}$ is $–(V_o–V_{\rm CB2} + n_2DV_{\rm in}/(1–D))$, the magnetizing current i_{m2} and the diode current i_{Do2} are given by

$$i_{m2}(t) = -I_{m22} + \frac{DV_{\rm in}}{L_{m2}(1-D)}(t - t_5) \tag{17}$$

$$i_{Do2}(t) = i_{\rm CB2}(t) = I_{Do2} - \frac{V_o - V_{\rm CB2} + (n_2 DV_{\rm in}/(1-D))}{L_{k2}}(t - t_5). \tag{18}$$

Mode 7 [t_6, t_7]: At t_6, the current $i_{\rm CB2}$ changes its direction. The output diode current i_{Do2} decreases to zero and the diode D_{o2} is turned OFF. Then the output diode D_{o1} is turned ON and its current increases linearly. Similar to D_{o1}, the current changing rate of D_{o2} is controlled by the leakage inductance L_{k2} of the transformer *T* and its reverse-recovery problem is alleviated. Since v_{p2} is the same as in Mode 6 and $v_{\rm Lk}2$ is $V_{\rm CB2}– n_2DV_{\rm in}/(1–D)$, the current i_{m2} and the diode current i_{Do2} are given by

$$i_{m2}(t) = i_{m2}(t_6) + \frac{DV_{\rm in}}{L_{m2}(1-D)}(t - t_6) \tag{19}$$

$$i_{Do1}(t) = -i_{\rm CB2}(t) = \frac{V_{\rm CB2} - (n_2 DV_{\rm in}/(1-D))}{L_{k2}}(t - t_6). \tag{20}$$

The currents i_{p2} and i_L can be obtained from the same relations in Mode 2. In this mode, the voltages v_{p1} and $v_{\rm Lk1}$ are equal to those in Mode 6. Therefore, the magnetizing current i_{m1}, the auxiliary current $i_{\rm Da}$, and the input current $i_{\rm in}$ change with the same slopes as in Mode 2.

III. Characteristic and Design Parameters

A. Voltage Gain of the Boost Converter Stage

Referring to the voltage waveform v_{p1} in Fig. 3, the volt-second balance law gives

$$V_{\rm in} DT_s - (V_{\rm dc} - V_{\rm in})(1-D)T_s = 0. \tag{21}$$

From (21), the voltage gain of the proposed ZVS boost converter stage is obtained by

$$\frac{V_{\rm dc}}{V_{\rm in}} = \frac{1}{1-D} \tag{22}$$

which is the same as that of the conventional CCM boost converter.

B. Auxiliary Diode Current Reset Timing Ratio d_1

By applying the volt-second balance law to the voltage waveform $v_{\rm Lk1}$, the auxiliary diode current reset timing ratio d_1 is determined by

$$d_1 = \frac{n_1 D(1-D)}{n_1(1-D)+1}. \tag{23}$$

C. Maximum Auxiliary Diode Current $I_{\rm Da}$

From Modes 6 and 7, the maximum auxiliary diode current $I_{\rm Da}$ is obtained by

$$I_{\rm Da} = \frac{n_1 DV_{\rm in} T_s}{L_{k1}}. \tag{24}$$

D. DC-Blocking Capacitor Voltage $V_{\rm CB1}$

Referring to the voltage waveform v_{p2} in Fig. 3, the volt-second balance law gives

$$V_{\rm CB1}(1-D)T_s - (V_{\rm dc} - V_{\rm CB1})DT_s = 0. \tag{25}$$

From (22) and (25), the dc-blocking capacitor voltage $V_{\rm CB1}$ is obtained by

$$V_{\rm CB1} = \frac{DV_{\rm in}}{1-D}. \tag{26}$$

E. Maximum Output Diode Currents I_{Do1} and I_{Do2}

From Modes 2 and 7, the maximum output diode current I_{Do1} can be written as follows:

$$I_{Do1} = \frac{n_2 V_{\rm in} + V_{\rm CB2}}{L_{k2}} d_2 T_s = \frac{-V_{\rm CB2} + (n_2 DV_{\rm in}/(1-D))}{L_{k2}} \times ((1-D) - d_3)T_s. \tag{27}$$

From Modes 3, 4, and 6, the maximum output diode current I_{Do2} can be written as follows:

$$I_{Do2} = \frac{n_2 V_{\rm in} + V_{\rm CB2} - V_o}{L_{k2}}(D - d_2)$$

$$T_s = \frac{V_o - V_{\rm CB2} + (n_2 DV_{\rm in}/(1-D))}{L_{k2}} d_3 T_s. \tag{28}$$

F. Output Voltage V_{o2} of the Half-Bridge Converter Stage

From (27) and (28), the dc-blocking capacitor voltage $V_{\rm CB2}$ and the output voltage V_o can be derived as follows:

$$V_{\rm CB2} = \frac{D - d_2 - (D/(1-D))d_3}{1 - D + d_2 - d_3} \cdot n_2 V_{\rm in} \tag{29}$$

$$V_o = \frac{D - d_2 - (D/(1-D))d_3}{(D - d_2 + d_3)(1 - D + d_2 - d_3)} \cdot n_2 V_{\rm in}. \tag{30}$$

G. Output Diode Current Reset Timing Ratios d_2 and d_3

Since the average value of the current $i_{\rm CB2}$ should be zero, the following relation can be obtained:

$$(1 - D + d_2 - d_3) I_{Do1} = (D - d_2 + d_3) I_{Do2}. \tag{31}$$

From (27) to (31), the relation between d_2 and d_3 is obtained by

$$\frac{d_2}{d_3} = \frac{D}{1-D}. \tag{32}$$

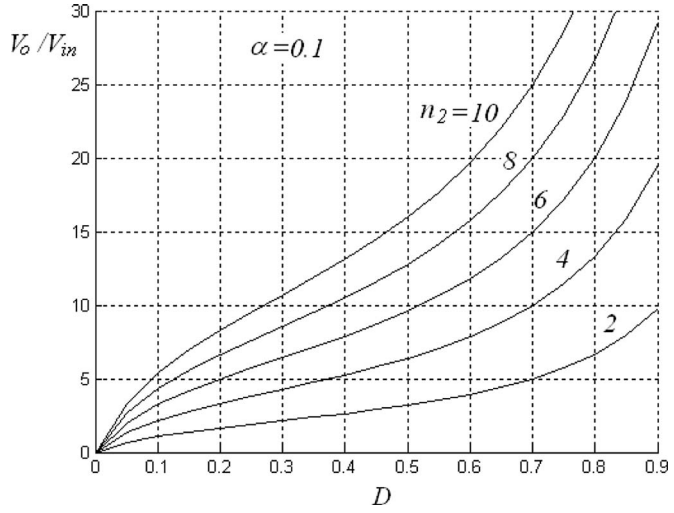


Fig. 5 Voltage gain according to *D* under $\alpha = 0.1$ and different n_2 values.

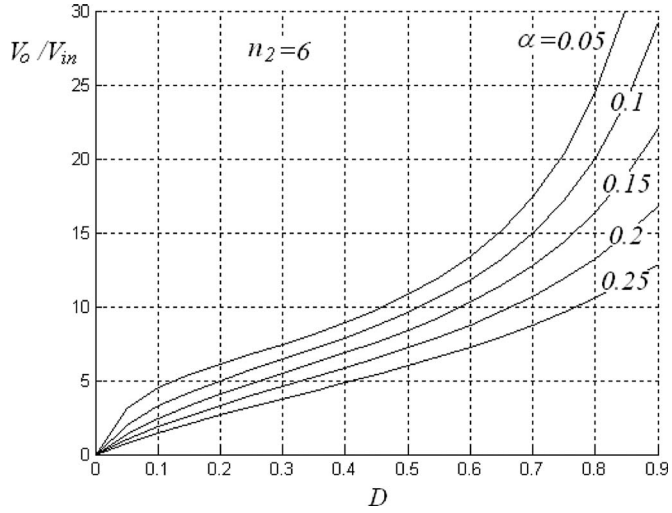


Fig. 6 Voltage gain according to *D* under $n_2 = 6$ and different α values.

Since the average value of the current i_{m2} is zero, its peak values I_{m21} and I_{m22} have the same value as follows:

$$I_{m21} = I_{m22} = \frac{DV_{\rm in}T_s}{2L_{m2}}. \tag{33}$$

From Fig. 2, the output current I_o can be represented by

$$I_o = (1 - D + d_2 - d_3)\frac{I_{Do1}}{2} = (D - d_2 + d_3)\frac{I_{Do2}}{2}. \tag{34}$$

From (27), (28), (32), and (34), d_2 and d_3 are obtained by

$$d_2 = \alpha D \tag{35}$$

$$d_3 = \alpha(1 - D) \tag{36}$$

$$\alpha = \frac{1}{2}\left(1 - \sqrt{1 - \frac{8L_{k2}I_o}{n_2 V_{\rm in} D T_s}}\right). \tag{37}$$

H. Voltage Gain M of the Proposed DC–DC Converter

From (22), (30), (35), and (36), the voltage gain *M* of the proposed converter is given by

$$M = \frac{V_o}{V_{\rm in}} = \frac{n_2 D(1 - 2\alpha)}{(D(1 - 2\alpha) + \alpha)(1 - \alpha - (1 - 2\alpha)D)}. \tag{38}$$

Figs. 5 and 6 show the voltage gain *M* according to the duty cycle *D*. In Fig. 5, the voltage gain *M* under $\alpha = 0.1$ and several n_2 values is shown. As n_2 increases, the voltage gain *M* increases. In Fig. 6, the voltage gain *M* under $n_2 = 6$ and several α values is shown. As α increases, the voltage gain *M* decreases. Namely, larger L_{k2} reduces the voltage gain *M*. Since α depends on I_o, $V_{\rm in}$, and *D*, Figs. 5 and 6 can be used in obtaining n_2 and α only at the maximum duty cycle under the full load condition.

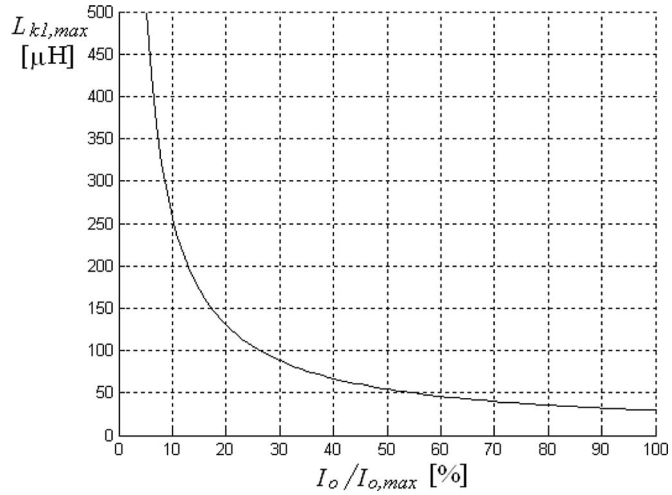


Fig. 7 Maximum leakage inductance $L_{k1,\max}$ for ZVS.

I. Input Current Ripple

The input current ripple $\Delta i_{\rm in}$ can be written by

$$\Delta i_{\rm in} = I_{m11} - I_{m12} + n_1 I_{\rm Da} = \frac{n_1^2 L_{m1} + L_{k1}}{L_{m1}L_{k1}} \cdot DV_{\rm in}T_s. \tag{39}$$

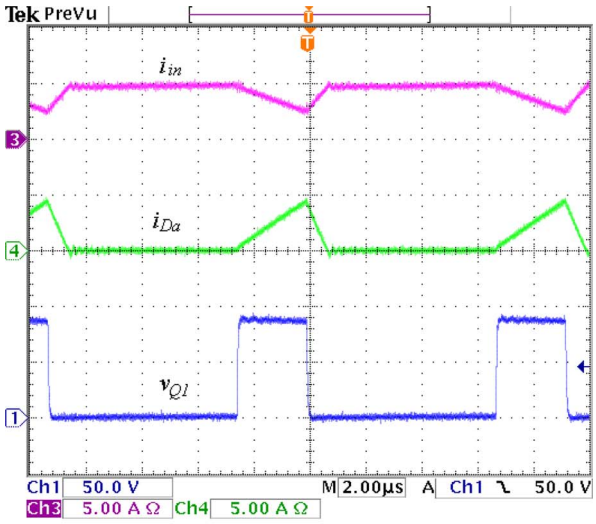
To reduce the input current ripple below a specific value $I*$, the magnetizing inductance L_{m1} should satisfy the following condition:

$$L_{m1} > \frac{1}{(I^*/DV_{\rm in}T_s) - \left(n_1^2/L_{k1}\right)}. \tag{40}$$

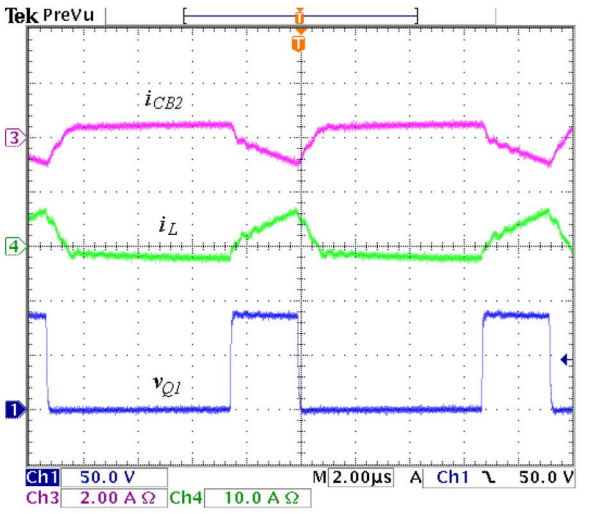
J. ZVS Conditions

As is seen in Fig. 3, both the boost converter stage and the half-bridge converter stage have ZVS function. From Fig. 3, the ZVS condition for Q_2 is given by

$$I_{m11} + I_{L2} = I_{m11} + I_{m22} + n_2 I_{Do2} > 0. \tag{41}$$



(a)



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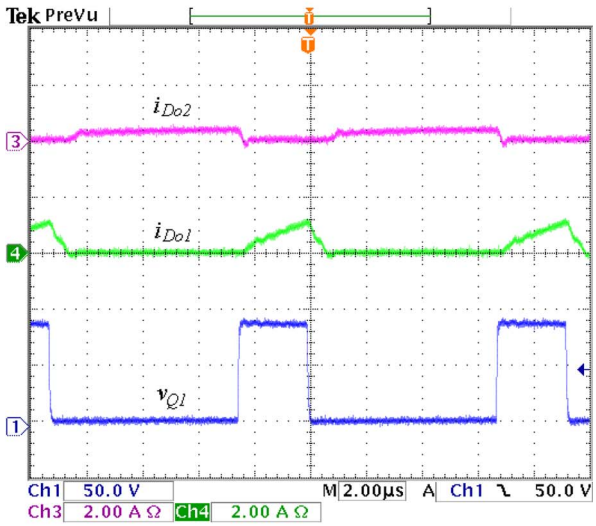
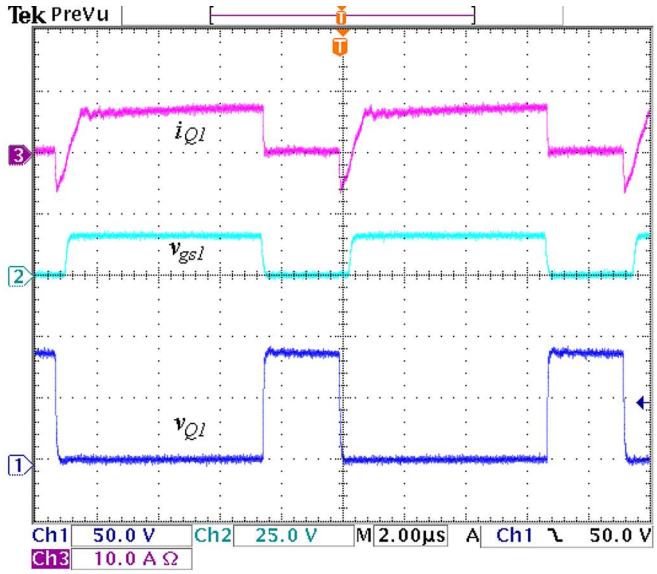
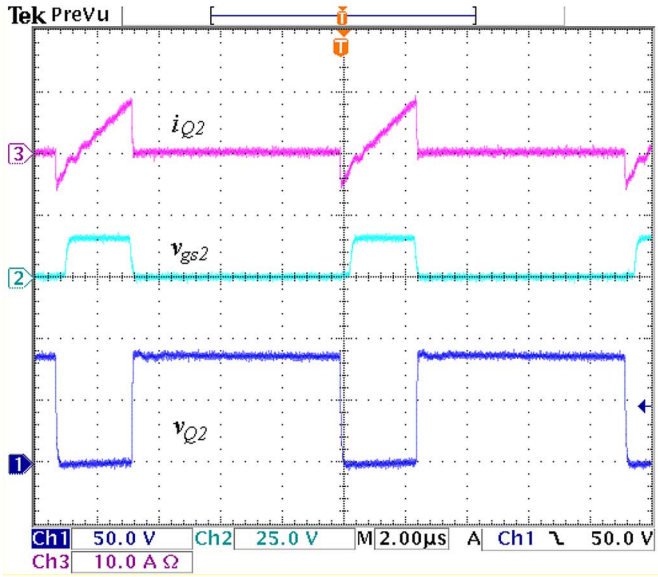


(c)

Fig. 8 Experimental waveforms. (a) $i_{\rm in}$, $i_{\rm Da}$, and v_{Q1}. (b) $i_{\rm CB2}$, i_L, and v_{Q1}. (c) i_{Do1}, i_{Do2}, and v_{Q1}.



(a)



(b)

Fig. 9 Experimental waveforms. (a) i_{Q1}, $v_{\rm gs1}$, and v_{Q1}. (b) i_{Q2}, $v_{\rm gs2}$, and v_{Q2}.

Since the current values I_{m11}, I_{m22}, and I_{Do2} have positive values, the ZVS condition for Q_2 is always satisfied. Similarly, for ZVS of Q_1, the following condition should be satisfied:

$$I_{m21} + n_2 I_{Do1} + (n_1 + 1)\, I_{\rm Da} - I_{m12} > 0. \tag{42}$$

The terms I_{m21} and $n_2 I_{Do1}$ are from the half-bridge converter stage and the terms $(n_1 + 1) I_{\rm Da}$ and I_{m12} are from the boost converter stage. If the boost converter stage is designed to satisfy the above inequality (42) regardless of the status of the half-bridge converter stage, ZVS of the proposed converter is always accomplished. In this case, the leakage inductance L_{k1} of the coupled inductor L_c should satisfy the following condition:

$$L_{k1} < \frac{(n_1 + 1)\, n_1 D V_{\rm in} T_s}{P_o / V_{\rm in}} \tag{43}$$

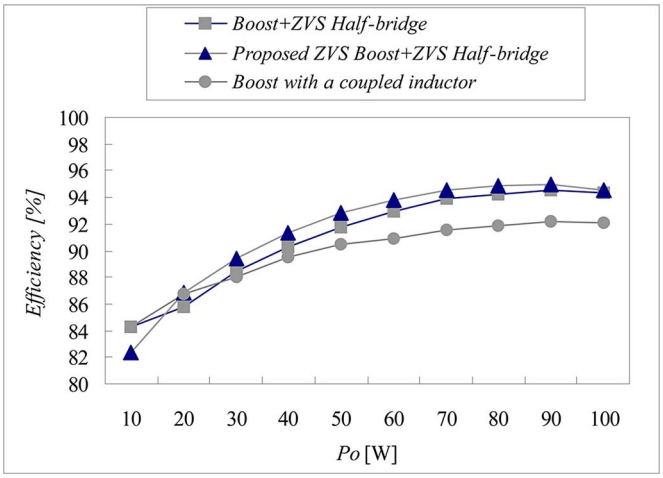


Fig. 10 Measured efficiency.

where P_o is the output power and the minimum value I_{m12} of the magnetizing current i_{m1} is approximated as $P_o/V_{\rm in}$.

IV. Experimental Results

To verify the theoretical analysis of the proposed dc–dc converter, a 100 W prototype is implemented. The input voltage $V_{\rm in}$ and the output voltage V_o are 24 V and 393 V, respectively. The switching frequency f_s is 108 kHz. According to the design parameters given in Section III, the circuit parameters can be selected. The turn ratio n_1 of the coupled inductor L_c is calculated from (23). By choosing a proper d_1, the turn ratio n_1 can be determined. Here, d_1 is chosen as 0.88 and n_1 is selected as $n = 0.5$. From Figs. 5 and 6, α and n_2 are selected as 0.1 and 6, respectively. From (43), the leakage inductance L_{k1} of the coupled inductor L_c can be determined. Fig. 7 shows the maximum leakage inductance $L_{k1,\max}$ according to normalized output current. In order to obtain ZVS regardless of the load condition, L_{k1} needs to be designed to satisfy the ZVS condition at full load. From Fig. 7, L_{k1} is selected as 16.75 μH. Then the magnetizing inductance L_{m1} is designed as 800 μH form (40) with $I* = 2.7$ A. According to α, the leakage inductance L_{k2} of the transformer T is selected as 170 μH. The magnetizing inductance L_{m2} of the transformer T is selected as 474 μH. The dc-blocking capacitors C_{B1} and C_{B2} are 6.6 μF and 2.2 μF, respectively. The aluminum electrolytic capacitors 470 μF/100 V and 47 μF/450 V are used as the dc-link capacitor $C_{\rm dc}$ and the output capacitor C_o, respectively.

Fig. 8 shows the experimental waveforms of the prototype. In Fig. 8(a), the input currents $i_{\rm in}$, the auxiliary diode current $i_{\rm Da}$, and the voltage v_{Q1} across the lower switch. Since the input current $i_{\rm in}$ does not change its direction, the proposed converter operates in CCM. The dc-link voltage $V_{\rm dc}$ is around 85 V. Therefore, the voltage stresses of the power switches are confined to 85 V. Fig. 8(b) shows the currents i_L and $i_{\rm CB2}$. It can be seen that the experimental waveforms agree with the theoretical analysis. In Fig. 8(c), the output diode currents i_{Do1} and i_{Do2} are shown. It is clear that the reverse-recovery current is significantly reduced due to the leakage inductance L_{k2} of the transformer T. Fig. 9(a) and (b) shows ZVS operations of Q_1 and Q_2. In Fig. 9(a), the voltage v_{Q1} across the switch Q_1 goes to zero due to the negative direction of the switch current before the gate pulse $v_{\rm gs1}$ for the switch Q_1 is applied to Q_1. Since the voltage v_{Q1} across the switch Q_1 goes to zero before the gate pulse is applied to the switch, the switch Q_1 operates with ZVS. Similarly, Fig. 9(b) shows the ZVS operation of the lower switch Q_2. In Fig. 9, there is no surge current at the moments that the switches Q_1 and Q_2 are turned ON. The measured efficiency is shown in Fig. 10. The proposed ZVS dc–dc converter exhibits an efficiency of 94.5% at the full load condition. The efficiency was improved by 2.4% compared with the conventional nonisolated boost converter with a coupled inductor for a high voltage gain [8]. In addition, the efficiency of the modified version of the proposed converter is plotted. In the modified version, the input stage of the proposed converter is changed with the conventional CCM boost converter and the half-bridge converter stage is redesigned. The efficiency of the proposed converter with the ZVS boost converter stage is higher than those of the others under from 20% to 100% load. However, the efficiency of the proposed converter at light load is lower due to the additional conduction loss of the auxiliary circuitry of the ZVS boost converter stage.

V. Conclusion

A ZVS dc–dc converter with high voltage gain was suggested. It can achieve ZVS turn-ON of two power switches while maintaining CCM. In addition, the reverse-recovery characteristics of the output diodes were significantly improved by controlling the current changing rate with the use of the leakage inductance of the transformer. The proposed converter presents a higher efficiency and a wider ZVS region compared to other soft-switching converters due to the ZVS boost converter stage.

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