Voltage Gain Enhancement for Step-Up Converter Constructed by KY and Buck-Boost Converters

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Abstract—In this paper, a novel voltage-boosting converter is presented, which combines one charge pump and one coupled inductor with the turns ratio. The corresponding voltage gain is greater than that of the existing step-up converter combining KY and buck-boost converters. Since the proposed converter possesses an output inductor, the output current is non-pulsating. After some mathematical deductions, an experimental set-up with 12V input voltage, 72V output voltage, and 60W output power is used to verify the effectiveness of the proposed converter.

Keywords—KY converter, charge pump, coupled inductor.

I. INTRODUCTION

Because of the global warming, the demand of the green power has been increasing for decades. These kinds of green power facilities include solar cells, fuel cells, etc. In many applications, high voltage conversion converters play an important role in boosting the low output voltages of green power facilities to the high voltages which the loads need. Regarding the traditional non-isolated voltage-boosting converters [1], [2], such as the traditional boost converter and buck-boost converter, their voltage gains are not high enough. Up to now, many kinds of voltage-boosting techniques have been presented, including several inductors which are magnetized and then pump the stored energy into the output with all inductors connected in series [3], coupled inductors with turns ratios [4]-[8], [10], [11], [15], voltage superposition based on switching capacitors [9], [13]-[18], auxiliary transformers with turns ratios [12], etc. In [8] and [10], the output terminal is floating, thereby increasing application complexity. In [4]-[11], [16] and [17] these converters contain too many components, thereby making the converters relatively complicated. In [3]-[11], [15], [16] and [17], the output currents are pulsating, therefore causing the output voltage ripples to tend to be large. In [12], [13], [14] and [18] even though the output currents are non-pulsating, their voltage gains are not high enough. As described in the appendix, Table III makes a comparison between the converters shown in the references, in terms of voltage gain, component number, switch voltage stress, output inductor and floating output.

Based on the mentioned above, a novel step-up converter is presented. This converter combines one KY converter [12], one traditional synchronously rectified (SR) buck-boost converter, and one coupled inductor with the turns ratio, which is used to improve the voltage gain. Therefore, the voltage gain is higher than that of the converter in [14] and can be determined by adjusting both the duty cycle and the turns ratio. Besides, the duty cycle and the turns ratio are independent, which means that tuning the duty cycle does not affect the turns ratio and vice versa. In addition, the proposed step-up converter has no floating output, and has an output inductor so the output current is non-pulsating. Furthermore, part of the leakage inductance energy can be recycled to the output capacitor of the SR buck-boost converter. In this paper, a detailed description along with some experimental results is given to provide the effectiveness of the proposed converter.

II. OVERALL SYSTEM CONFIGURATION

Fig. 1 shows the proposed converter, which contains two MOSFET switches $S_1$ and $S_2$, one coupled inductor composed of the primary winding with $N_p$ turns and the secondary winding with $N_s$ turns, one energy-transferring capacitor $C_1$, one charge pump capacitor $C_2$, one diode $D_1$, one output inductor $L_o$, and one output capacitor $C_o$. In addition, the input voltage is denoted by $V_i$, the output voltage is signified by $V_o$, and the output resistor is represented by $R_o$.

III. BASIC OPERATING PRINCIPLES

Before taking up this section, there are some assumptions to be made as follows.

1. The coupled inductor is modeled as an ideal transformer except that one magnetizing inductor $L_m$ is connected in parallel with the primary winding and one leakage inductor $L_l$ is connected in series with the primary winding. Therefore, the coupling coefficient $k$ is defined as $k = L_m / (L_m + L_l)$.

2. The proposed converter operates in the positive current mode. That is, the currents flowing through the magnetizing inductor $L_m$ and the output inductor $L_o$ are always positive.

3. The dead times between the two MOSFET switches are omitted.
(4) The MOSFET switches and the diodes are assumed to be ideal components.
(5) The values of all the capacitors are large enough such that the voltages across them are kept constant at some values.
(6) The magnitude of the switching ripple is negligible.

Therefore, the small ripple approximation will be adopted herein in analysis.

The following analysis contains the explanation of the power flow path for each mode, along with the corresponding equations and voltage gain. Inherently, there are two operating modes in the proposed converter. And, the gate driving signals $v_{gs1}$ and $v_{gs2}$ of the two switches $S_1$ and $S_2$ have the duty cycles of $(1-D)$ and $D$, respectively, where $D$ is the dc quiescent duty cycle created from the controller. In addition, the input current is denoted by $i_i$, the current through the $N_p$ winding is signified by $i_{Np}$, the current through the $N_i$ winding is represented by $i_{Nim}$, the current through $L_m$ is denoted by $i_{Lm}$, the current through $R_s$ is signified by $i_s$. On the other hand, the voltage across $L_m$ or the voltage across the $N_i$ winding is signified by $v_{Nip}$, the voltage across the $N_i$ winding is represented by $v_{Nim}$, the voltage across $C_1$ is indicated by $V_{C1}$, the voltage across $C_2$ is denoted by $V_{C2}$, and the voltage across $L_o$ is described by $v_{Lo}$.

$\text{Fig. 2. Key waveforms of the proposed converter.}$

$\text{Fig. 3. Power flow in mode 1 with coupling coefficient equal to one.}$

$\text{A. Voltage Gain Considering Coupling Coefficient Equal to One}$

In this case, the coupling coefficient $k$ is equal to one, that is, the leakage inductor is omitted. Besides, the key waveforms of the proposed converter with two operating modes are shown in Fig. 2.

1) Mode 1: During this interval, as shown in Fig. 3, $S_1$ is turned off, but $S_2$ is turned on. Therefore, the input voltage $V_i$ is imposed on $N_p$, thus causing $L_m$ to be magnetized and the voltage across $N_i$ to be induced, equal to $V_i \times N_i / N_p$. In addition, $D_1$ becomes forward-biased, $C_2$ is charged to $V_i + V_{C1} + V_{Lm} - V_o$, and the voltage across $L_o$, $v_{Lo}$, is a negative value, equal to $V_{C2} - V_o$, thus making $L_o$ demagnetized. As a consequence, the input voltage $V_i$, together with the voltage across $C_1$, $V_{C1}$, plus the induced voltage on $N_i$, $v_{Nim}$, plus the voltage across $L_m$, $v_{Lo}$, provides the energy to the load. Also, the associated equations are shown below:

$$v_{Np} = V_i$$  \hspace{1cm} (1)
$$v_{Lo} = V_{C2} - V_o$$  \hspace{1cm} (2)

$\text{Fig. 3. Power flow in mode 1 with coupling coefficient equal to one.}$

2) Mode 2: During this interval, as shown in Fig. 4, $S_1$ is turned on, but $S_2$ is turned off. Therefore, the voltage $-V_{C1}$ is imposed on $N_p$, thereby causing the magnetizing inductor $L_m$ to be demagnetized, and the voltage across $N_i$ to be induced, equal to $-V_{C1} \times N_i / N_p$. In addition, $D_1$ becomes reverse-biased, the voltage on $L_o$ is a positive value, equal to $V_i + V_{C1} + V_{C2} - V_o$, thus causing $L_o$ to be magnetized. As a result, the input voltage $V_i$, together with the voltage across $L_m$, $v_{Np}$, plus the voltage across $C_2$, $V_{C2}$, provides the energy to $L_o$ and the load. Also, the corresponding equations are shown below:

$$v_{Np} = -V_{C1}$$  \hspace{1cm} (3)
$$v_{Lo} = V_i + V_{C1} + V_{C2} - V_o$$  \hspace{1cm} (4)

By applying the voltage-second balance principle to $L_m$ over one switching period, the following equation can be obtained:

$$V_i \times D + (-V_{C1}) \times (1-D) = 0$$  \hspace{1cm} (5)

Also, by rearranging the above equation, the voltage across $C_1$, $V_{C1}$, can be obtained as follows:

$$V_{C1} = \frac{D}{1-D} \times V_i$$  \hspace{1cm} (6)

Likewise, by applying the voltage-second balance principle to $L_o$ over one switching period, the following equation can be obtained:
\[(V_{C2} - V_o) \times D + (V_i + V_{C1} + V_{C2} - V_o) \times (1 - D) = 0 \]  
(7)

The voltage across \(C_2\), \(V_{C2}\), can be represented by
\[V_{C2} = V_i + V_{C1} + V_i \times \frac{N_s}{N_p} \]  
(8)

Next, based on (6), (7) and (8), the corresponding voltage gain can be expressed to be
\[\frac{V_o}{V_i} = \frac{2 - D}{1 - D} \times \frac{N_s}{N_p} \]  
(9)

From (9), it can be seen that \(0 < D < 1\).

Next, substituting (12) and (17) into (18) yields the voltage gain:
\[\frac{V_a}{V_i} = \frac{2 - D + k \frac{N_s}{N_p}}{1 - D} \]  
(19)

Fig. 7 shows the curves of voltage gain versus duty cycle of the proposed converter, considering different values of coupling coefficient \(k\) with the same turns ratio \(n (= N_s/N_p)\) set to three. Fig. 8 depicts the curves of voltage gain versus duty cycle of the proposed converter, considering different turns ratios with the same coupling coefficient set to one. Fig. 9 illustrates the voltage gain of the proposed converter versus duty cycle of the proposed converter without any negative

2) Mode 2: During this interval, as shown in Fig. 6, the voltages across \(L_o\) and \(C_1\) is to be expressed as follows. Above all, part of the energy stored in \(L_o\) and \(L_{11}\) can be transferred to \(C_1\). Hence, the corresponding equations are shown below:
\[v_{N_p} = -kV_{C1} \]  
(14)
\[v_{L_o} = V_i + V_{C1} + V_{C2} - V_o \]  
(15)

By applying the voltage-second balance to both \(L_o\) and \(L_{11}\) over one switching period, one can get
\[V_i \times D + (-V_{C1}) \times (1 - D) = 0 \]  
(16)

Sequentially, by rearranging the above equation, the voltage across \(C_1\), \(V_{C1}\), can be obtained to be
\[V_{C1} = \frac{D}{1 - D} \times V_i \]  
(17)

Likewise, by applying the voltage-second balance principle to \(L_o\) over one switching period, the following equation can be obtained to be
\[(V_{C2} - V_o) \times D + (V_i + V_{C1} + V_{C2} - V_o) \times (1 - D) = 0 \]  
(18)

Next, substituting (12) and (17) into (18) yields the voltage gain:
\[\frac{V_a}{V_i} = \frac{2 - D + k \frac{N_s}{N_p}}{1 - D} \]  
(19)
magnetizing inductor current and any negative output inductor current, as compared with the traditional boost converter in [1] and the converter in [14].

![Fig. 7. Curves of voltage gain versus duty cycle for the proposed converter with different values of coupling coefficient $k$ but the same turns ratio $n$.](image)

![Fig. 8. Curves of voltage gain versus duty cycle for the proposed converter with different values of turns ratio $n$ but the same coupling coefficient $k$.](image)

![Fig. 9. Comparison of voltage gain versus duty cycle for three types of converters.](image)

**C. Boundary Condition for Magnetizing Inductor**

The condition for the magnetizing inductor $L_m$ operating in what region will be described as follows:

\[
\begin{align*}
2I_{L_m} & \geq \Delta I_{L_m}, \text{ for all current values in the positive current region} \\
2I_{L_m} & < \Delta I_{L_m}, \text{ for part of current values in the negative current region}
\end{align*}
\]

(20)

where $I_{L_m}$ and $\Delta I_{L_m}$ are the dc and ac components of $i_{L_m}$, respectively.

The expression of $I_{L_m}$ can be obtained from (21) to (24). For analysis convenience, it is assumed that the input power is equal to the output power. According to the voltage-second balance for the inductor and the ampere-second balance for the capacitor, the dc component of the inductor voltage and the dc component of the capacitor current are zero. Therefore, as shown in Fig. 10, from the dc component of $i_{N_s}$, $I_{N_s}$, is equal to the output current $I_o$. Likewise, as shown in Figs. 10 and 11, the current $I_i$ entering into the primary side of the coupled inductor, is the dc component of $i$, and is equal to the dc component of $i_{N_p}$, $I_{N_p}$, plus the dc component of $i_{L_m}$, $I_{L_m}$. Therefore,

\[
I_i = \frac{2-D}{1-D} \times \frac{V_o}{R_o} \times I_o
\]

(21)

\[
I_{N_p} = \frac{N_s}{N_p} \times I_{N_s} = \frac{N_s}{N_p} \times I_o
\]

(22)

\[
I_{L_m} = I_i - I_{N_p} = \frac{2-D}{1-D} \times \frac{V_o}{R_o} \times I_o
\]

(23)

In Fig. 11, $I_o$ can be expressed as $V_o/R_o$. Substituting $V_o/R_o$ for $I_o$ in (23) yields the following equation:

\[
I_{L_m} = \frac{2-D}{1-D} \times \frac{V_o}{R_o}
\]

(24)

Also, $\Delta I_{L_m}$ can be represented by

\[
\Delta I_{L_m} = \frac{V_o D T}{L_m} \times \frac{I_{N_s}}{I_o}
\]

(25)

As $2I_{L_m} \geq \Delta I_{L_m}$, $L_m$ operates in the positive current region. Moreover, the further deduction is shown as follows:

\[
2I_{L_m} \geq \Delta I_{L_m}
\]

\[
\Rightarrow 2 \times \frac{2-D}{1-D} \times \frac{V_o}{R_o} \geq \frac{V_o D T}{L_m}
\]

\[
\Rightarrow 2L_m \geq \Delta I_{L_m} \geq \frac{D(1-D)^2}{R_o T_s} \times (2 + n - D - nD)(2 - D)
\]

(26)
\[ K_1 \geq K_{\text{crit}}(D) \]
where \( K_1 = \frac{2I_m}{R_o T_s} \) and \( K_{\text{crit}}(D) = \frac{D(1-D)^2}{(2+n-D-nD)(2-D)} \).

From (26), the relationship between \( K_{\text{crit}}(D) \) and \( D \) is shown in Fig. 12 under the condition that \( n \) is set at three. From Fig. 12, it can be seen that if \( K_{\text{crit}}(D) \) is larger than \( K_1 \), \( L_m \) will operate in the positive current region; otherwise, part of \( i_{L_m} \) will enter into the negative current region.

![Fig. 12. Boundary condition for magnetizing inductor \( L_m \).](image)

**D. Boundary Condition for Output Inductor**

The conditions for the output inductor \( L_o \) operating in what region will be described as follows:

\[ \begin{align*}
2I_{L_o} &\geq \Delta i_{L_o}, \text{for all current values in the positive current region} \\
2I_{L_o} &< \Delta i_{L_o}, \text{for part of current values in the negative current region}
\end{align*} \quad (27) \]

where \( I_{L_o} \) and \( \Delta i_{L_o} \) are the dc and ac components of \( i_{L_o} \), respectively.

Since \( I_{L_o} \) is equal to \( I_o \), replacing \( I_o \) with \( V_o/R_o \) yields the following equation:

\[ I_{L_o} = \frac{V_o}{R_o} \quad (28) \]

Also, \( \Delta i_{L_o} \) can be expressed by

\[ \Delta i_{L_o} = \frac{V_o \Delta M}{L_o} = \frac{(V_f + V_{C1} + V_{C2} - V_o) \times (1-D) T_s}{L_o} \quad (29) \]

Inserting equations (4), (6) and (7) into (29) yields the following equation:

\[ \Delta i_{L_o} = \frac{V_o D T_s}{L_o} \quad (30) \]

As \( 2I_{L_o} \geq \Delta i_{L_o} \), \( L_o \) operates in the positive current region. In addition, the more deduction is shown as follows:

\[ \begin{align*}
2I_{L_o} &\geq \Delta i_{L_o} \\
\Rightarrow 2I_o &\geq \frac{V_o D T_s}{L_o} \\
\Rightarrow 2I_o &\geq \frac{D(1-D)}{2+n-D-nD} \\
\Rightarrow K_2 &\geq K_{\text{crit2}}(D)
\end{align*} \quad (31) \]

where \( K_2 = \frac{2I_o}{R_o T_s} \) and \( K_{\text{crit2}}(D) = \frac{D(1-D)}{2+n-D-nD} \).

From (31), the relationship between \( K_{\text{crit2}}(D) \) and \( D \) is shown in Fig. 13. From Fig. 13, it can be seen that if \( K_{\text{crit2}}(D) \) is larger than \( K_2 \), \( L_o \) will operate in the positive current region; otherwise, part of \( i_{L_o} \) will enter into the negative current region.

![Fig. 13. Boundary condition for output inductor \( L_o \).](image)

**IV. CONTROL METHOD APPLIED WITH DESIGN CONSIDERATIONS**

Fig. 14 shows the overall system block diagram. First of all, the voltage divider transfers the output voltage to a desired lower value, which is fed to the analog-to-digital converter (ADC) to create a corresponding digital signal. After this, this digital signal is sent to the field programmable gate array (FPGA), which is the control kernel, containing one serial peripheral interface (SPI), one proportional-integral (PI) controller, and one digital pulse-width modulation (DPWM) generator. Eventually, the FPGA processes this digital signal, and accordingly produces two gate driving signals to drive the MOSFET switches. The system specifications and used component names of the proposed converter are shown in Tables I and II, respectively. Besides, the PI controller design method is referred to page 95 of the technical report [19]. There are two steps to tune the parameters of the proportional gain \( k_p \) and the integral gain \( k_i \) in the PI controller as follows.

1. **Step 1:** Starting with \( k_p \neq 0 \) and \( k_i = 0 \), and trimming \( k_p \) until a small residual error is received.
2. **Step 2:** Increasing \( k_i \) until the system reaches an almost zero final error.
current when the output current is above 20%–30% of the rated output current [20]. Therefore, in this paper, the boundary between the positive current and the negative current is assumed to be at 20% of the rated output current. Hence, the value of $L_o$ can be obtained as follows:

$$L_o = \frac{v_o \Delta t}{\Delta I_{o,\text{rated}}} \approx \frac{(V_o + V_{C1} + V_{C2} - V_o)(1-D) T_o}{\Delta I_{o,\text{rated}}}$$

$$= \frac{(V_o + V_{C1} + V_{C2} - V_o)(1-D) T_o}{20\% \times I_{o,\text{rated}} \times 2 \times (12 + 12 \times 0.5 + 12 \times 3 - 72)(0.5 \times 10 \mu F)} = 180 \mu F$$

Eventually, the value of $L_o$ is set at 189\mu H.

B) Capacitor Design

1) Energy-transferring capacitor design: Assuming the peak-to-peak value of the capacitor voltage during the charge period, $\Delta V_{C1}$, is set to 1% of $V_{C1}$ or less, that is, $\Delta V_{C1}$ is smaller than 120mV, the value of $C_1$ can be obtained as follows:

$$C_1 \geq \frac{i_{C1} \Delta t}{\Delta V_{C1}} = \frac{(I_{o,\text{rated}} - I_{o,\text{rated}})(1-D)T_o}{0.01 \times V_{C1}}$$

$$\Rightarrow C_1 \geq \frac{(5 - 0.833)(1 - 0.5) \times 10 \mu F}{0.01} \approx 174 \mu F$$

where $I_{o,\text{rated}}$ is the dc input current $I_o$ under rated conditions. And eventually, two 470\mu F capacitors with positive terminals connected in series are selected for $C_1$ [21].

2) Charge pump capacitor design: Assuming the variation in capacitor voltage during the discharge period, $\Delta V_{C2}$, is set to 0.1% of $V_{C2}$ or less, that is, $\Delta V_{C2}$ is smaller than 60mV, the value of $C_2$ can be obtained as follows:

$$C_2 \geq \frac{i_{C2} \Delta t}{\Delta V_{C2}} = \frac{I_{o,\text{rated}}(1-D) T_o}{0.01 \times V_{C2}} \approx 0.001 \times V_{C2}$$

$$\Rightarrow C_2 \geq \frac{0.833 \times (1 - 0.5) \times 10 \mu F}{0.001 \times 60} \approx 69.4 \mu F$$

where $I_{o,\text{rated}}$ is the dc current in $L_o$ under rated conditions. And finally, two 47\mu F capacitors connected in parallel are chosen for $C_2$ [21].

3) Output capacitor design: As generally known, the output filter is used to filter out the output current ripple as much as possible. Prior to designing $C_o$, the output voltage ripple $\Delta V_o$ is assumed to be smaller than 0.1% of the rated output voltage, that is, $\Delta V_o$ is smaller than 72mV. Therefore, the equivalent series resistance of the output capacitor, $ESR$, can be represented by

$$ESR \leq \frac{\Delta V_o}{\Delta I_{o,\text{rated}}} \approx \frac{0.001 \times V_{C2}}{0.01 \times 72} = 0.216 \Omega$$

Besides, a rule of thumb for the electrolytic capacitor [2] is

How to design the magnetizing inductor $L_{mn}$, the energy-transferring capacitor $C_1$, the charge pump capacitor $C_2$, the output capacitor $C_o$ and the output inductor $L_o$ is shown as follows.

A) Inductor Design

1) Magnetizing inductor design: To make sure that $L_{mn}$ always operates in the positive region, the required equation is as follows.

$$L_{mn} \geq \frac{V \Delta T}{2 \times I_{mn,\text{min}}} = \frac{V \Delta T}{2 \times 0.5 \times 10 \mu F} = 100 \mu H$$

where $I_{mn,\text{min}}$ is the minimum dc current in $L_{mn}$. And finally, the value of $L_{mn}$ is set at 148.7\mu H.

2) Output inductor design: From the industrial viewpoint, the output inductor is generally designed to have no negative

Table I System specifications of the proposed converter

<table>
<thead>
<tr>
<th>System parameters</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage ($V_i$)</td>
<td>12V</td>
</tr>
<tr>
<td>Rated output voltage ($V_o$)</td>
<td>72V</td>
</tr>
<tr>
<td>Rated output current ($I_{o,\text{rated}}$) power ($P_{o,\text{rated}}$)</td>
<td>0.833A/60W</td>
</tr>
<tr>
<td>Minimum output current ($I_{o,\text{min}}$) power ($P_{o,\text{min}}$)</td>
<td>0.1A/7.2W</td>
</tr>
<tr>
<td>Switching frequency ($fs$)</td>
<td>100kHz</td>
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</tbody>
</table>

Table II Components used in the proposed converter

<table>
<thead>
<tr>
<th>Components</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET switches $S_1$, $S_2$</td>
<td>STP120NF, $V_{FQ}=100V$, $I_{FQ}=120A$, $R_{on}=10.5\Omega$</td>
</tr>
<tr>
<td>Diode $D_1$</td>
<td>V20120C, $V_{FQ}=120V$, $I_{FQ}=20A$, $V_{FQ}=0.54V$, $I_{FQ}=5A$</td>
</tr>
<tr>
<td>Energy-transferring capacitor $C_1$</td>
<td>Two 470\mu F/50V Rubycon capacitors with positive terminals connected in parallel</td>
</tr>
<tr>
<td>Charge pump capacitor $C_2$</td>
<td>Two 470\mu F/100V MIEC capacitors connected in parallel</td>
</tr>
<tr>
<td>Output capacitor $C_o$</td>
<td>Two 220\mu F/100V MIEC capacitors connected in series</td>
</tr>
<tr>
<td>Coupled inductor</td>
<td>Core: PTS40/27/3C02, $N_1=N_2=13$, $L_{o}=148.7 \mu H$, $L_{o}=3.0 \mu H$, $k=0.997$</td>
</tr>
<tr>
<td>Output inductor $L_o$</td>
<td>Core: ER40/20/13, $N_o=20$, air-gap of 0.35mm, $L_{o}=189 \mu H$</td>
</tr>
<tr>
<td>FPGA</td>
<td>EP1C3T100</td>
</tr>
<tr>
<td>Half-bridge gate driver</td>
<td>IR2011</td>
</tr>
<tr>
<td>ADC</td>
<td>ADC7476</td>
</tr>
</tbody>
</table>
\[ C_o \times ESR = 65\mu \]  
(37)

Therefore, based on (36) and (37), the value of \( C_o \) can be represented by
\[
C_o \geq \frac{65\mu}{ESR} \approx 300\mu F
\]

(38)

Eventually, two 220 \( \mu F \) capacitors connected in parallel are selected for \( C_o \) [21].

V. EXPERIMENTAL RESULTS

Figs. 15 to 17 show the measured waveforms at light load, namely, \( I_o = 0.1A \). Fig. 15 shows the gate driving signal for \( S_1 \), \( v_{gs1} \), the gate driving signal for \( S_2 \), \( v_{gs2} \), the current passing through the primary side of the coupled inductor, \( i_{Np}+i_{Lm} \), and the current passing through the secondary side of the coupled inductor, \( i_{Ns} \). Fig. 16 shows the gate driving signal for \( S_1 \), \( v_{gs1} \), the gate driving signal for \( S_2 \), \( v_{gs2} \), the voltage across \( L_o \), \( V_{Lo} \), and the current through \( L_o \), \( i_{Lo} \). Fig. 17 shows the gate driving signal for \( S_1 \), \( v_{gs1} \), the gate driving signal for \( S_2 \), \( v_{gs2} \), the voltage across \( C_1 \), \( V_{C1} \), and the voltage across \( C_2 \), \( V_{C2} \). On the other hand, Figs. 18 to 20 show the same measured waveform items as those for Figs. 15 to 17, except for half load, namely, \( I_o = 0.4A \), whereas Figs. 21 to 23 show the same waveform items as those for Figs. 15 to 17, except for rated load, namely, \( I_o = 0.833A \).

From the waveforms mentioned above, the proposed converter can stably operate all over the load range. Moreover, from Fig. 16, it can be seen that there is a negative current in \( L_o \). Furthermore, the heavier the load is, the higher the voltages across \( C_1 \) and \( C_2 \). This is because the voltages across \( C_1 \) and \( C_2 \) are functions of the duty cycle \( D \). That is, as the output current increases, the output voltage will decrease. Therefore, in order to maintain the output voltage at the constant value, the feedback control system will increase \( D \). Consequently, the voltages across \( C_1 \) and \( C_2 \) will increase as well.

On the other hand, Figs. 24 and 25 show the currents through \( S_1 \) and \( S_2 \) and the voltages across \( S_1 \) and \( S_2 \) at rated load. Without the voltage spikes considered, the measured voltage stresses of \( S_1 \) and \( S_2 \) are both about 27V, which is somewhat different from the ideal value of 24V. This is because the voltage drops due to parasitic impedance makes the duty cycle bigger than the ideal value. Without the currents spikes considered, the measured current stresses of \( S_1 \) and \( S_2 \) are about 3A and 10A, respectively. Furthermore, Figs. 26 and 27 show the waveforms of output voltage and current in the steady state at rated load, and in the transients from light/rated load to rated/light load, respectively. From Fig. 27, it can be seen that the output voltage undershoot due to the load change from light load to rated load is about 4.7V with the corresponding recovery time of about 225ms, whereas the output voltage overshoot due to the load change from rated load to light load is about 4.3V with the resulting recovery time of about 240ms.

Aside from these, Fig. 28 shows the curve of efficiency versus load current. From Fig. 28, it can be seen that the efficiency all over the load range is above 88%, and the maximum efficiency can be up to 95%.
Fig. 18. Waveforms at half load: (1) $v_{g1}$; (2) $v_{g2}$; (3) $i_{Np} + i_{Lm}$; (4) $i_{Np}$.

Fig. 19. Waveforms at half load: (1) $v_{g1}$; (2) $v_{g2}$; (3) $v_{L0}$; (4) $i_{L0}$.

Fig. 20. Waveforms at half load: (1) $v_{g1}$; (2) $v_{g2}$; (3) $V_{C1}$; (4) $V_{C2}$.

Fig. 21. Waveforms at rated load: (1) $v_{g1}$; (2) $v_{g2}$; (3) $i_{Np} + i_{Lm}$; (4) $i_{Np}$.

Fig. 22. Waveforms at rated load: (1) $v_{g1}$; (2) $v_{g2}$; (3) $v_{L0}$; (4) $i_{L0}$.

Fig. 23. Waveforms at rated load: (1) $v_{g1}$; (2) $v_{g2}$; (3) $V_{C1}$; (4) $V_{C2}$. 
VI. CONCLUSION

A novel high step-up converter is presented herein. By combining the coupled inductor with the turns ratio, and the switched capacitor, the corresponding voltage gain is higher than that of the existing step-up converter combining KY and buck-boost converters. Furthermore, the proposed converter has no floating output, and has one output inductor so the output current is non-pulsating. Moreover, the structure of the proposed converter is quite simple and very suitable for industrial applications.

APPENDIX

Table III makes a comparison between the converters shown in the References, in terms of voltage gain, component number, switch voltage stress, output inductor and floating output.
Table III Comparison between the converters shown in the References, in terms of voltage gain, component number, switch voltage stress, output inductor and floating output

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Voltage gain</th>
<th>Component number</th>
<th>Switch voltage stress</th>
<th>Output inductor</th>
<th>Floating output</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3]</td>
<td>( \frac{1}{(1-D)^2} )</td>
<td>8</td>
<td>( V_{d1} = \frac{V_I}{1-D}, V_{d2} = V_{d3} = \frac{V_I}{(1-D)^2} )</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[4]</td>
<td>( \frac{1+n}{1-D} )</td>
<td>10</td>
<td>( V_{d1} = nV_I, V_{d2} = \frac{nD}{1-D} V_I )</td>
<td>No</td>
<td>No</td>
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<tr>
<td>[5]</td>
<td>( \frac{2+n}{1-D} )</td>
<td>10</td>
<td>( V_{d1} = \frac{V_I}{1-D} )</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[6]</td>
<td>( \frac{1+n}{1-D} )</td>
<td>15</td>
<td>( V_{d1} = \frac{V_I}{1-D} )</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[7]</td>
<td>( \frac{2}{1-D} + nD )</td>
<td>13</td>
<td>( V_{s1} = V_{s2} = \frac{V_o}{2} - \frac{nDV_I}{2} )</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[8]</td>
<td>( \frac{1+D+nD}{1-D} )</td>
<td>9</td>
<td>( V_{d1} = \frac{V_I}{1-D} )</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>[9]</td>
<td>( \frac{2-D}{1-D} )( \frac{n}{n: \text{stage number}} )</td>
<td>12, ( n=2 ) 18, ( n=3 )</td>
<td>( \frac{2-D}{1-D} )( \frac{n}{n} )</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[10]</td>
<td>( \frac{2(1+nD)}{1-D} )</td>
<td>10</td>
<td>( V_{d1} = \frac{(1+nD)}{1-D} V_I )</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>[11]</td>
<td>( \frac{2+nD}{1-D} )</td>
<td>14</td>
<td>( V_{d1} = \frac{V_o}{2} - \frac{nDV_I}{2(1-D)} )</td>
<td>No</td>
<td>No</td>
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<tr>
<td>[12]</td>
<td>( \frac{1+D}{1-D} )</td>
<td>6</td>
<td>( V_{d1} = 2V_I, V_{d2} = V_I )</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>[13]</td>
<td>( \frac{2-D}{1-D} )</td>
<td>8</td>
<td>( V_{d1} = V_{d2} = \frac{V_I}{1-D} )</td>
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<td>[14]</td>
<td>( \frac{2-D}{1-D} )</td>
<td>8</td>
<td>( V_{d1} = V_{d2} = \frac{V_I}{1-D} )</td>
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<td>[15]</td>
<td>( \frac{2}{1-D} + n )</td>
<td>8</td>
<td>( V_{d1} = V_{d2} = \frac{V_I}{1-D} )</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[16]</td>
<td>Type 1: ( \frac{3-D}{1-D} ) Type 2: ( \frac{2}{1-D} ) Type 3: ( \frac{3-2D}{1-D} )</td>
<td>10</td>
<td>Type 1: ( V_{d1} = V_{d2} = V_I ) ( V_{d3} = V_o - 2V_I ) Type 2: ( V_{d1} = V_{d2} = V_I ) ( V_{d3} = V_o - V_I ) Type 3: ( V_{d1} = V_{d2} = V_I ) ( V_{d3} = V_o - V_I )</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[17]</td>
<td>( \frac{2nD}{1-D} + 1 )</td>
<td>11</td>
<td>( V_{d1} = V_I, V_{d2} = V_I ) ( V_{d3} = \frac{3D-1}{1-D} V_I )</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[18]</td>
<td>Type 1: ( 2D ) Type 2: ( 2D )</td>
<td>8</td>
<td>Type 1: ( V_{d1} = V_I, V_{d2} = V_I ) ( V_{d3} = V_I, V_{d4} = V_I ) Type 2: ( V_{d1} = V_I, V_{d2} = V_I ) ( V_{d3} = V_I, V_{d4} = V_I )</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
REFERENCES


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