Novel Two Stage Buck-Boost Converter with Zero-Voltage Transition Operation

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Abstract— **This paper proposes a soft switching technique in a novel two stage buck-boost converter comprising from two identical separate units. The converter units are connected to each other by an interleaved inductor. The soft switching method utilized is Zero Voltage Transition which means turning on the switches while the voltage applied on them is equal to zero. This operation is done with establishing the gate pulses of the converter switches at the accurate time intervals. The soft switching operation of the converters has significantly effect in reducing the switching losses of the circuit, and causes an effective increment in the converter efficiency. This paper describes the procedure of the circuit operation to obtain the correct performance of the proposed converter. The simulation results have been done in the PSPICE software and depicted the accuracy of performing the ZVT method.**

Keywords-component; two stage buck-boost Converter, Interleaved Inductor, Zero Voltage Transition (ZVT)

I. INTRODUCTION

The main application of step-down/up converters is in regulated dc power supplies, where a negative-polarity output may be desired with respect to the common terminal of the input voltage and the output voltage can be either higher or lower than the input voltage [1-3]. A buck-boost converter can be obtained by the cascade connection of the two basic converters: the step-down converter and the step-up converter. A perfect description of the buck-boost converter has been represented in [4].

Converter efficiency is one of the most important practical ends. Many soft switching techniques are proposed in the literatures to achieve the minimum switching losses and more efficiency in DC/DC converters. Some of these methods contain synchronous rectification technique utilize replacing the freewheeling diode current by active power switches [5-7]. This technique requires one more inductor and auxiliary active power switch moreover the main switches. Another scheme like auxiliary active snubbers are also proposed to reduce the switching losses in [8], and active-clamp circuits in [9], [10] are also useful. Recently, soft switching techniques have been proposed where utilize the features of zero-voltage switching (ZVS) or zero-current switching (ZCS) for the DC/DC converters. These methods substantially reduce the switching losses, and hence attain high efficiency as well as the switching frequency is increases. The resonant ZVS and ZCS converters represented earlier, create high voltage stress on the switches. Therefore, snubber circuits were required to prevent the active switches from possible damages [11].

Zero voltage transition (ZVT) with interleaved inductor between two parallel converters is one another effective technique to reduce the switching losses and voltage stress on the switches. This method, perform the switching while the voltage applied on the switches is almost equal to zero. The main idea of this technique is reducing the switching losses which are form a great part of the total losses, and followed significantly improvement in converter efficiency. Two step-down and step-up DC/DC converters that accomplish ZVT operation are presented in [12] and [13]. Moreover, converters with interleaved operation are general nowadays; For example interleaved boost converters that are applicable as power-factor-correction circuits represented in [14-15]. An interleaved converter with a coupled winding is proposed to reduce the losses of the clamp circuits in [16-17]. In addition, by adopting two power converters which working in parallel, some other advantages are resulted than utilizing a single converter with the same specification, such as the capability of supplying more output power and providing lower output voltage and input current ripple.

This paper describes the procedure of achieving the soft switching operation of a novel proposed interleaved buck-boost converter. This task is obtained because of resonating between the intrinsic capacitors of the switches and the interleaved inductor which placed among two units. Thus, the ZVT operation of the switches is obtained and the converter efficiency could experiences more improvement than a similar converter with hard switching utilization. Operation analysis of the converter circuit has been clarified in eight modes.

The paper is organized as follows: circuit configuration and discussion is described in Section II. Circuit operation analysis discussed in Section III. Considerations on circuit design are outlined in Section IV. Simulation results are presented in Section V and finally the paper is concluded in Section VI.

II. CIRCUIT CONFIGURATION AND DISCUSSION

Fig. 1 shows the configuration of the proposed converter. In this structure an interleaved inductor L_S has been placed among the two converter units. This element plays an important role in the main idea of the ZVT soft switching manner, called zero voltage transition. It is because that the interleaved inductor L_S and the intrinsic capacitances of the switches form a resonating circuit. Therefore the resonating current causes the intrinsic capacitors to be discharged and the voltage clamped on the switches become equal to zero. Thus, the switches can pass through the off state to on at zero voltage and the ZVT operation of the proposed converter is obtained.

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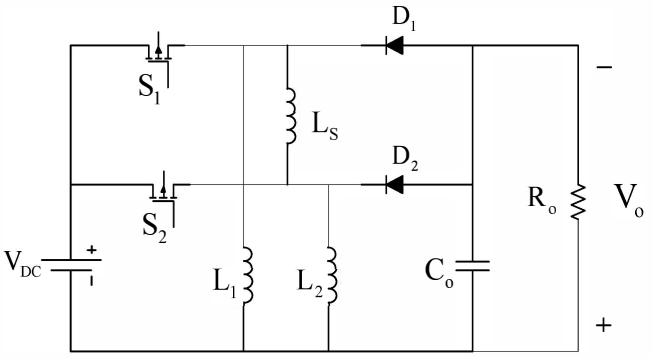

Figure 1. Proposed two stage buck-boost converter.

Two power MOSFETs S_1 and S_2 are adopted for high frequency switching. The switching frequency for both MOSFETs is equal to f_S. In this method, the switching gate signals should have very small overlapping intervals to displacing the remaining of the resonating current between the switches. Therefore, the duty ratio has been chosen slightly greater than 0.5 to create these overlapping intervals. To minimize the ripples in the input current and output voltage the converter operate in Continuous Current Mode (CCM). The output capacitor C_O is common between two converters and assumed to be very large to stabilize the output voltage.

The equivalent circuit which is shown in Fig. 2 has been used to describe the procedure of the proposed two stage buck-boost converter. To simplifying the analysis, it could be assumed that the currents of the inductors L_1 and L_2 are constant at the CCM; So, they have been modeled by a constant current source as shown in Fig. 2. The detailed model of the active power switches has been considered. It comprises from an intrinsic antiparallel body diode and parasitic capacitances in parallel with an ideal switch.

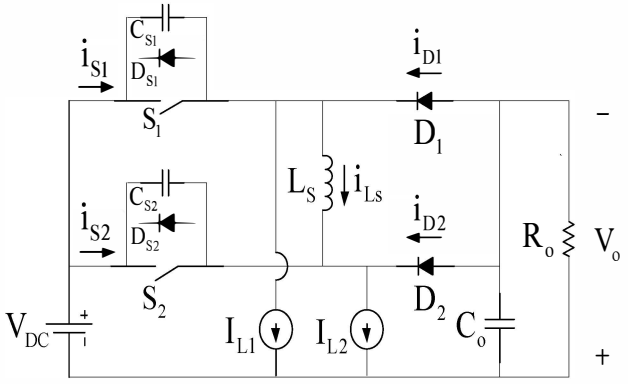

Figure 2. Equivalent circuit diagram of the proposed converter.

III. CIRCUIT OPERATION ANALYSIS

The operation procedure of the converter has been represented in eight modes depends on the different statues of the elements. Because of the two buck-boost converters are completely identical, all of the circuit elements such as L_1, L_2, C_{S1} and C_{S2} have the same values. In all of these modes, the forward voltage drops on the diodes D_1, D_2 and switches S_1, S_2 considered to be negligible. The equivalent circuit of each mode of operation has been shown in Fig. 3.

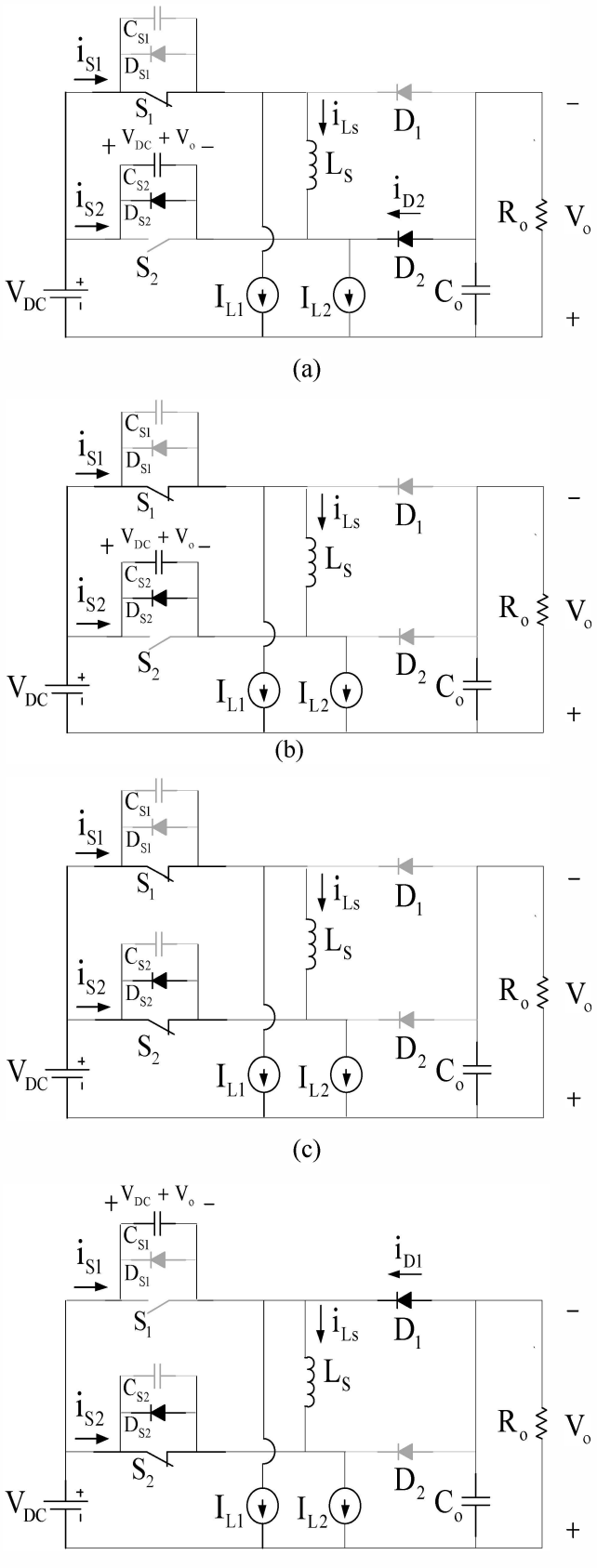

Figure 3. Equivalent circuit diagrams in different operation modes. (a) mode I, (b) mode II, (c) mode III, (d) mode IV.

Mode I— $t_0 < t < t_1$: mode I begins when D_2 freewheeling current which is equal to I_{L2} decreasing to zero. Before entering this mode the switch S_2 has been turned off while S_1 has been turned on. Therefore, the voltage $V_{DC}+V_O$ which was clamped on the capacitor C_{S2} in the previous mode, imposes on the interleaved inductor L_S. Thus, the inductor current i_{Ls} increased up linearly from $-I_{L1}$ to I_{L2} meanwhile the S_1 current increases linearly from a small negative current go through the D_{S1}. When i_{Ls} rises up to I_{L2}, S_1 current reaches to $I_{L1}+I_{L2}$. In whole of this process V_{CS2} considered to be constant at $V_{DC}+V_O$.

Mode II— $t_1 < t < t_2$: this mode starts when the freewheeling current of D_2 reaches to zero. Therefore L_S and C_{S2} form a resonant circuit and a resonant current rises up between them. So the capacitor C_{S2} which was clamped at $V_{DC}+V_O$ as initial voltage before entering this mode, begins to discharge by the resonant current until it reaches to zero voltage. Then, D_{S2} will be forward biases to conduct the resumption of the resonant current cycle. Now both the resonant current and the inductor current I_{L2} flow through the interleaved inductor L_S, therefore the current i_{Ls} becomes a little larger than I_{L2}.

Mode III— $t_2 < t < t_3$: at the beginning of this mode, V_{DS2} has been fixed at zero because D_{S2} conduct a small current which is the difference between i_{Ls} and I_{L2}. Therefore this is an appropriate opportunity to turning on the switch S_2 by applying the gating signal V_{GS2} during this interval. Thus, the switch S_2 could be turned on at the zero voltage.

Mode IV— $t_3 < t < t_4$: at the beginning of this mode, the switch S_1 is turned off. Therefore, the intrinsic capacitor C_{S1} charged up rapidly to $V_{DC}+V_O$, by sum of the currents I_{L2} and I_{L1}. Now, by applying a KVL in the upper loop of the circuit which has been depicted in Fig. 3 (d), the voltage on the diode D_1 becomes equal to zero. Therefore, it begins to freewheel the load current.

In the next interval, similar to mode I, V_{CS1} will be apply on the inductor L_S and the current i_{Ls} starts to be reversed contrary to mode I.

Since two buck-boost converters are identical, mode V to VIII have similar operation for switch S_1 zero turning on. The theoretical waveforms of each mode have been shown in Fig.-4.

IV. Circuit Design Considerations

It has been mentioned in section II that the duty ration of the converter switches should be slightly greater than 0.5 to create overlapping intervals between the gate signals. But, it can be implied from Fig. 4 that the effective duty ratio for either of the S_1 and S_2 is greater than the gate signals which are applied to them. Because, the effective turn off interval of the switches is only in mode V and I for conversion units I and II respectively. In fact, this time intervals are the periods where the diodes D_1 and D_2 are conducting. In other time intervals the switches S_1 and S_2 pass the load current or a small negative current which is the remaining of the same resonating current that flow through the antiparallel diodes D_{S1} and D_{S2}. As shown in Fig. 4, the modes I and V that are the time intervals for current commutation of the interleaved inductor L_s, is the

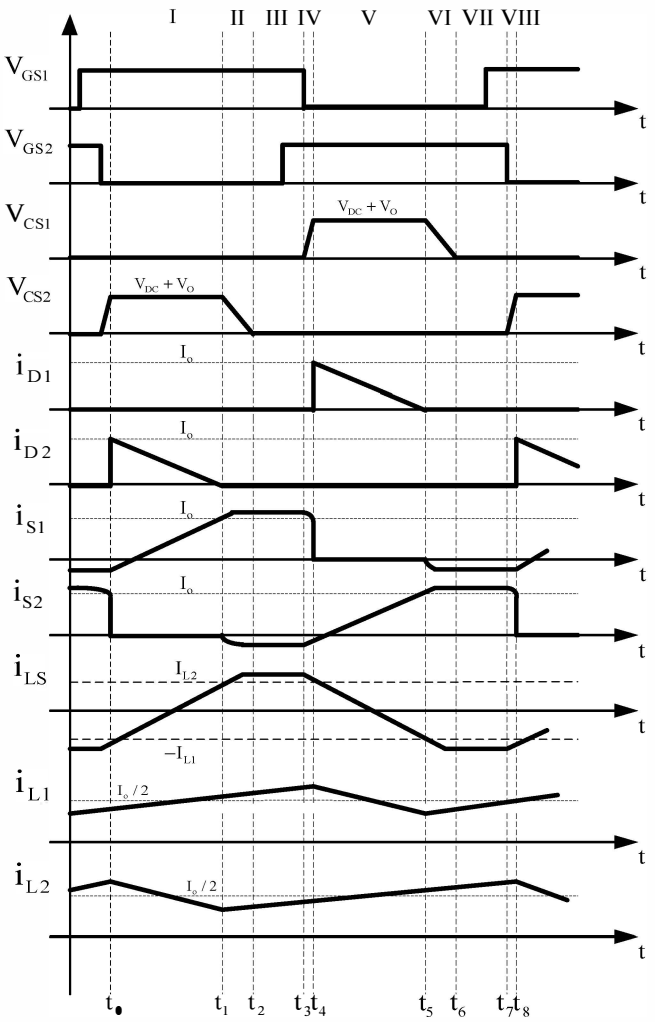

Figure 4. Theoretical waveforms.

effective turn off interval of each unit. Thus, the effective duty ratio can be represented as:

$$D_E = \frac{T_S - T_C}{T_S} \tag{1}$$

where T_S and T_C are the switching period and the commutation time of L_S, respectively.

Because the inductor current i_{Ls} approximately swings between values I_{L2} and I_{L1} during the modes I and V; And in these periods the voltage applied on the L_S is equal to $V_{DC}+V_O$, the commutation time can be obtained as bellows from (1). Also, the summation of I_{L2} and I_{L1} could be considered equal to $I_{in}+I_O$ in (2).

$$T_C = \frac{L_S(I_{L1}+I_{L2})}{V_{DC}+V_O} = \frac{L_S(I_{in}+I_O)}{V_{DC}+V_O} \tag{2}$$

According to the relationship between the output and input voltage and current of the buck-boost converter in the CCM, the commutation time can be resulted in terms of the output current, input voltage and the inductance L_S as follows:

$$T_C = \frac{D_E L_S}{V_{DC}} I_O \quad (3)$$

Combining (3) and (1), the effective duty ratio can be resulted as:

$$D_E = \frac{1}{1 + \frac{f_S L_S}{V_{DC}} I_O} \quad (4)$$

Substituting (4) in the voltage ratio of the buck-boost converter, the output voltage can be represented as follows:

$$V_O = \frac{D_E}{1 - D_E} V_{DC} = \sqrt{\frac{R}{f_S L_S}} V_{DC} \quad (5)$$

where f_S is switching frequency and the I_O considered to be V_O/R, that R is the load resistance. Therefore the output voltage can be controlled by modifying the switching frequency, not changing the duty ratio D such normal buck-boost converters.

The time period of modes I or V which has been considered as the effective turn off intervals, could be assumed $(1\text{-}D_E)T_S$. Also, the voltage that clamped at the inductor L_S is $V_{DC}+V_O$. So, equation (6) can be presented between the voltage and current of the inductor L_S at these intervals.

$$\frac{di_{Ls}}{dt} = \frac{I_{L1} + I_{L2}}{(1 - D_E)T_S} = \frac{V_{Ls}}{L_S} \quad (6)$$

As mentioned prior, the term $I_{L1}+I_{L2}$ would be equal to $I_{in}+I_O$. Therefore, simplifying (6) with replacing the relationships between the input/output voltage and current, the value of the inductance L_S could be presented as (7) for a specified input voltage.

$$L_S = \frac{(1 - D_E)V_{DC}}{f_S I_O} \quad (7)$$

To achieve the value of the inductances L_1 and L_2, the considerations on the ripple magnitude of I_{L1} and I_{L2} should be taking into account. Because the converter operates in the CCM, the maximum permissible ripple of the current should not exceed than the rated output current. Considering modes I and V, the voltage $-V_O$ has been applied on the inductances L_1 and L_2, thus I_{L1} and I_{L2} are decreasing. Therefore the value of the inductances L_1 and L_2 should meet the following constraint.

$$L_{1,2} > \frac{D_E V_{DC}}{f_S I_O} \quad (8)$$

To specifying the value of the output capacitor C_O, it has been considered that the relative output voltage ripple $\Delta V_O/V_O$ be less than 1% of the nominal output voltage. So, a 100 µF capacitor has been selected and placed in parallel with the load.

Table I. The values and types of the circuit elements.

Circuit Parameters	Value
Inductors L_1 and L_2	180 µH
Inductor L_S	30 µH
Capacitor C_O	100 µF
Mosfets type S_1, S_2	IRF 640
Diodes type	BYV32

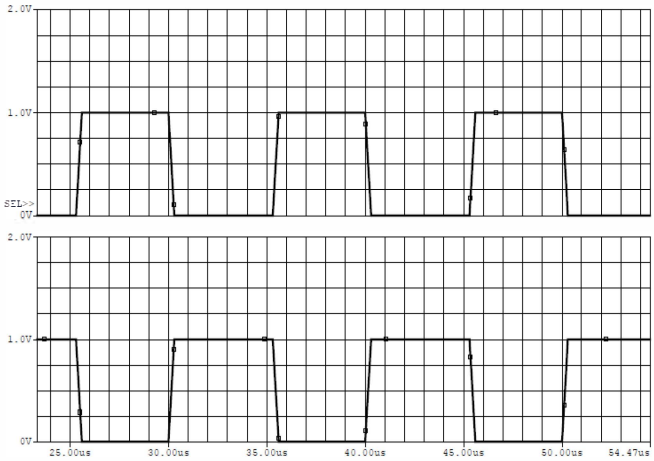

Figure 5. Gating signals of the switches.

V. SIMULATION RESULTS

To evaluate the applicability of the proposed converter, a similar structure has been simulated in the PSPICE software. The values of the circuit parameters and type of the elements have been listed in Table I. Fig. 5 shows the gate signals of the switches S_1 and S_2. The switching frequency has been considered 100 kHz. The input voltage selected a 50V DC source, so the output voltage has been fixed at 90V according to (5). The namely duty ratio of the switches has been considered 0.51 to create the overlapping intervals. Fig. 6 and 7 depicted the key component waveforms and the switch voltages of the converter. It could be concluded, that the performed analysis to achieve the ZVT operation of the converter has been verified, and the simulated waveforms are exactly adapted to the theoretical waveforms illustrated in Fig. 4. Thus, the switches can be turned on at the zero voltage and it means that the switching losses can be decreased. So it could be inferred that the proposed converter can develop significantly improvement in the converter efficiency. This should be investigated by experimental implementations and comparative studies between the proposed converter and a normal one stage buck-boost converter with the similar specifications.

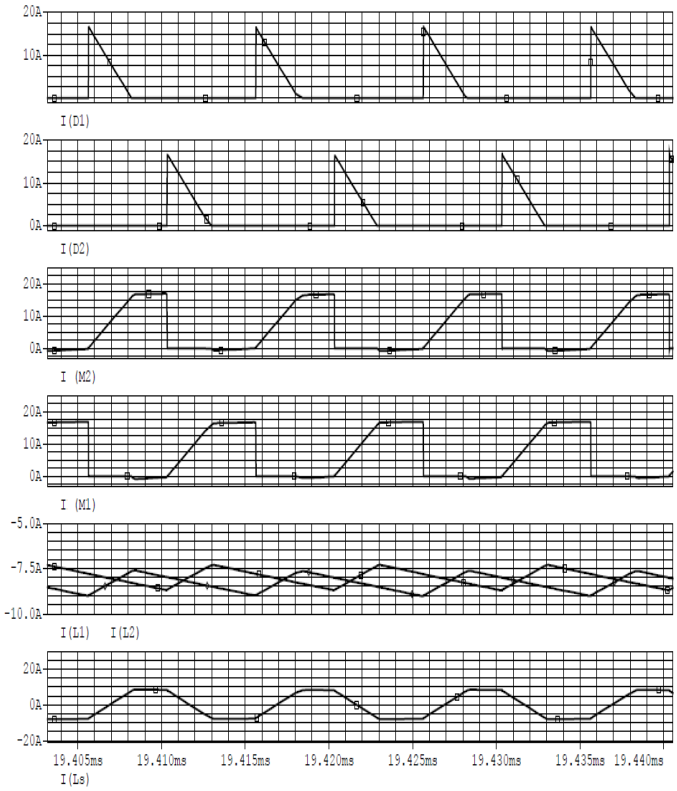

Figure 6. The currents of the circuit components.

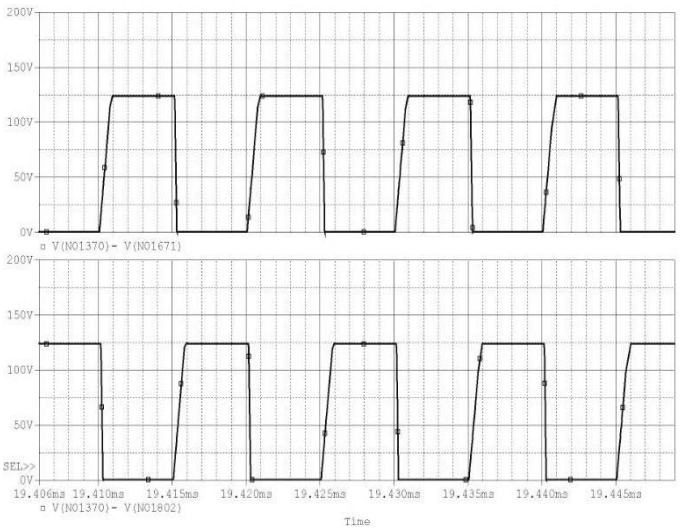

Figure 7. The voltage of the switches.

VI. CONCLUSION

In this paper, the ZVT operation of a novel two stage buck-boost converter comprises from two shunt identical buck-boost converters has been represented. The analysis and design considerations have been described. It has been illustrated that in the proposed converter the output voltage can regulate by varying the switching frequency instead of the duty ratio. To validate the performed analysis, a similar converter has been simulated and the results verified the performance of the proposed converter. It has been concluded that by applying the gate signals at the particular intervals, the switches can turn on at the zero voltage; Therefore, the converter efficiency can increases than a single converter with the same specifications. Moreover, another advantageous of the proposed converter could mention providing fewer ripples in the voltage and current of the load and input DC supply current, because of the parallel operation of two single converters.

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