Three-Phase *LLC* Series Resonant DC/DC Converter Using SiC MOSFETs to Realize High-Voltage and High-Frequency Operation

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***Abstract*—SiC MOSFETs are applied to constitute a three-phase, 5-kW *LLC* series resonant dc/dc converter with isolation transformers. A switching frequency of around 200 kHz for the transistors successfully reduces the volume of these isolation transformers, whereas insulated-gate bipolar transistors (IGBTs) are not capable of achieving such a high switching speed. The high-voltage tolerance of SiC MOSFETs, 1200 V, enables increasing the input voltage up to 600 V. High-voltage tolerance, on the other hand, is not compatible with low on-resistance for Si MOSFETs. A three-phase circuit topology is used to achieve up to 5 kW of power capacity for the converter and reduce per-phase current at the same time. Current-balancing transformers among these three phases effectively suppress a maximum peak current from arising in the circuit, a technique that miniaturizes the input and output capacitances. The conversion efficiency of the converter reaches 97.6% at 5-kW operation.**

***Index Terms*—Current-balancing transformers, *LLC* resonant converter, SiC MOSFETs, three phase, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

POWER electronics generally seek highly efficient and compact power conversion systems, and the switching power supply has been playing a significant role for this purpose. In a switching power conversion system, the two loss factors of switching devices, namely switching loss and conduction loss, mainly restrict the maximum conversion efficiency and consequently how much the losses are reduced depends on what switching devices are used and how to drive them.

One of the most important techniques to minimize switching loss is the so-called soft switching. Zero-voltage-switching (ZVS) pulsewidth modulation (PWM) converters typify power supply designs utilizing soft switching [1]. This circuit geometry efficiently reduces switching loss in a power circuit, but there still remain issues to be solved. For example, the reverse recovery of rectifier diodes generates voltage spikes, which often entail insufficient electromagnetic compatibility, the breakdown of dielectric substances in switching devices, and so on [2]. Many studies, of course, have already progressed to improve these disadvantages by appending auxiliary circuits [3]–[10], but these supplemental components make the whole system complicated, resulting in control difficulty and high production cost.

The *LLC* series resonant dc/dc converter (*LLC* dc/dc in short in the following paragraphs) is an attractive candidate circuit design [11]–[17] to bypass the aforementioned problems that ZVS PWM technology inevitably encounters. *LLC* dc/dc equipped with ZVS utilizes spontaneous resonance generated by the series connection of inductors and a capacitor (*LC* resonance), and hence quasi-sinusoidal current produced by the resonance prevents unexpected voltage spikes. This means that *LLC* dc/dc with ZVS and zero-current-switching (ZCS) demands no additional circuits, resulting in a simpler circuit design than ZVS PWM.

Utilization of spontaneous current resonance, however, restricts the latitude of switching devices. Transistors in *LLC* dc/dc should switch at high frequency because a high resonance frequency expands the adaptable range of output voltage [18] and downsizes passive components. Therefore, high-frequency switching devices such as SiC MOSFETs, GaN devices, and Si MOSFETs have advantages for setting up practical *LLC* dc/dc [19], whereas this requirement indicates that Si Insulated Gate Bipolar Transistors (IGBTs) are not good candidates for switching devices for *LLC* dc/dc due to their limited capability of switching speed.

We also have to accomplish power conversion efficiency as high as possible to fabricate an excellent *LLC* dc/dc. Low-voltage and high-current transfer of electric power generally deteriorates power conversion efficiency because of Joule heat loss as an inevitable consequence of large currents. Hence, electricity transfer with high voltage and low current is preferable to circumvent Joule heat loss. For this purpose, adoption of a three-phase topology and high input voltage are proper measures to reach high conversion efficiency. A three-phase configuration lessens circuit current per phase to 1/3 of the total current in an equivalent single-phase circuit. Accordingly, input and output current ripples can be reduced with capacitors only, while ZVS PWM needs *LC* filters for decreasing ripples [20].

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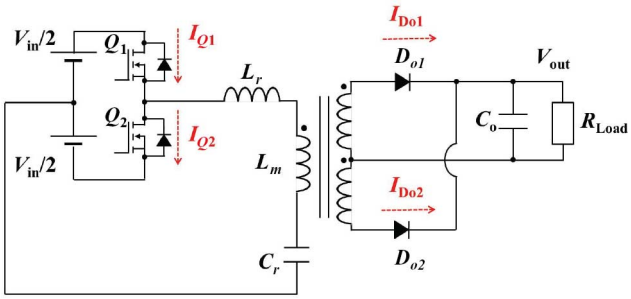

Fig. 1. Fundamental circuit of *LLC* dc/dc. V_{in}, V_{o}, and R_{load} denote input voltage, output voltage, and load resistance, respectively. C_{o} is the output capacitance. D_{o1} and D_{o2} are the rectifying diodes.

As for high input voltage, Si MOSFETs or GaN devices are not suitable as switching devices. These devices are superior to IGBTs in switching characteristics but possess a lower voltage tolerance than IGBTs. The tolerance of commercial Si MOSFETs and GaN devices is generally less than 650 V, and the versions of these devices that have breakdown-voltages (*BV*) over 650 V have ON-resistance R_{ON} that exceeds several hundred milliohms [21]–[22]. In addition, the voltage tolerance of power supplies must be larger than its input voltage for safe operation of the power system. Consequently, an input voltage over 600 V does not meet the general voltage tolerance of Si MOSFETs or GaN devices. Thus, for these devices, a feasible solution for a high input voltage option is a multilevel converter, in which switching devices share the high input voltage. This measure, however, needs many switching devices and also usually increases control system complexity and total fabrication cost [23]–[27].

On the other hand, SiC MOSFETs are capable of satisfying both requirements of high switching speed and high *BV* [28]. These advantageous device characteristics of SiC MOSFETs lead to effective miniaturization of *LLC* dc/dc with good power conversion efficiency through smaller transformers as a result of high switching speed and the adoption of high input voltage realized by high *BV*.

In this paper, the authors report the advantages of SiC MOSFETs with 1200-V *BV* to constitute a three-phase 5-kW *LLC* dc/dc with isolation transformers. Around 200 kHz, switching of the transistors successfully reduces the size of the isolation transformers which generally occupy a large volume of the power supply. The high *BV* allows large input voltage to over 600 V, and a three-phase configuration decreases the maximum current in the circuit, as a result of which the *LLC* dc/dc maintains practical power conversion efficiency. Furthermore, the additional transformers provide balance among these three-phase currents and suppress the maximum peak current in the circuit. This technique miniaturizes the input and output capacitances used. The conversion efficiency reaches 97.6% at 5-kW operation.

II. Operation Principle

The fundamental circuit of *LLC* dc/dc is shown in Fig. 1. The *LLC* circuit is basically composed of a half bridge which has two switches Q_1 and Q_2. These switches are connected with resonant inductance L_r, magnetizing inductance of isolation transformer L_m, and resonant capacitor C_r, and these passive components are configured as a resonant tank.

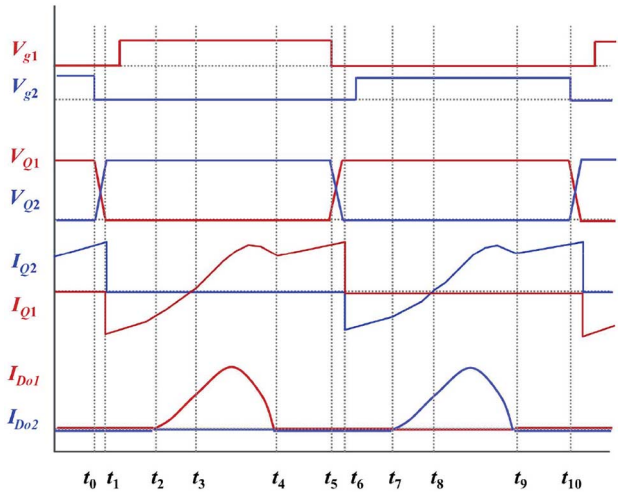

Fig. 2. Wave forms and timing chart of *LLC* dc/dc converter. Horizontal dashed lines represent zero level of each value.

Q_1 and Q_2 are alternately operated with a nearly 50% duty cycle. Dead times during turn-OFF of both Q_1 and Q_2 were set so as to avoid short circuit of Q_1 and Q_2. Q_1 and Q_2 are softly switched during the dead times as described below.

The timing chart of *LLC* dc/dc and its expected waveforms are displayed in Fig. 2. V_{gk}, V_{Qk}, and I_{Qk} denote gate–source voltage, drain–source voltage, drain current of Q_k, and I_{Dok} forward current of D_{ok}, respectively (for $k = 1,\ 2$). How the circuit operates is described as follows.

Term 1 $(t_0 - t_1)$: Term 1 begins with Q_2 turning OFF. V_{Q2} increases accompanying the resonance of $(L_m + L_r)$ and C_r during this term. This term lasts until V_{Q1} hits 0.

Term 2 $(t_1 - t_2)$: Term 2 starts when V_{Q1} reaches 0. The reverse current begins flowing through the body diode of Q_1. ZVS is achieved if Q_1 turns ON while this reverse current flows. The resonance of $(L_m + L_r)$ and C_r generates voltage in L_m so as for D_{o1} to be forwardly biased.

Term 3 $(t_2 - t_3)$: I_{Do1} begins flowing to resonate between L_r and C_r. This resonance increases I_{Do1} and electric power supplies the load.

Term 4 $(t_3 - t_4)$: Term 4 begins when I_{Q1} converts from a negative-to-positive value. During this term, I_{Do1} spontaneously decreases due to $L_r - C_r$ resonance. This term lasts until I_{Do1} reaches 0.

Term 5 $(t_4 - t_5)$: In this term, the resonance continues between $(L_m + L_r)$ and C_r. This term last until Q_1 turns OFF.

$(t_6 - t_{10})$: Terms 1–5 repeats with Q_1 and Q_2 exchanging their roles in the circuit.

III. Design of *LLC* Circuit

A. Experimental Circuit

The research team opted for a three-phase configuration with a mutual phase shift of 120° to improve efficiency [29]–[31].

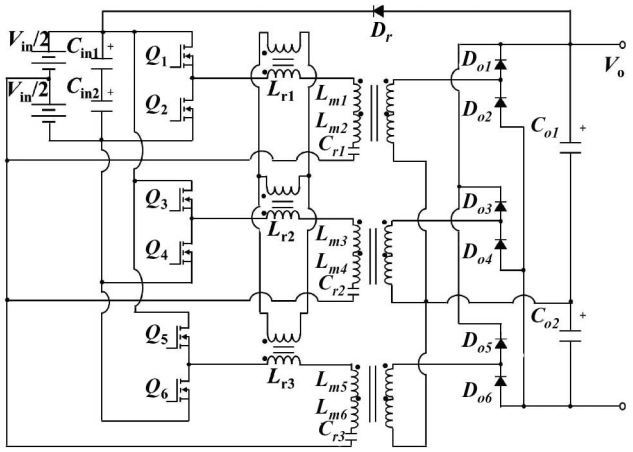

Fig. 3. Three-phase *LLC* dc/dc circuit. C_{in} and C_{o} denote input and output capacitance, respectively.

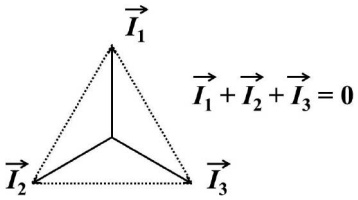

Fig. 4. Three-phase current-balancing topology.

Fig. 3 shows the three-phase *LLC* dc/dc equivalent circuit used for our study, and Q_j, D_{oj}, L_{mj} $(j = 1-6)$, and L_{ri}, C_{ri} $(i = 1-3)$ act the same as in Fig. 2.

Transformers showing the exact same characteristics are practically impossible to prepare and thereby current per phase inevitably deviates, aggravating output current ripples. Accordingly several methods to reduce this problem are proposed in [30] and [31], e.g., but these countermeasures demand external controllers. In order to avoid additional controllers, we put the parallel-connected transformers adjacent to L_{mbi} as shown in Fig. 3. These additional transformers are referred to as balanced transformers below. Balanced transformers act so as to equalize current of each phase, leading to miniaturization of input and output capacitors as detailed in Section IV-B. In addition, the suppression of peak currents provides a way to circumvent reliability deterioration of output capacitors [32].

The mutual phase shift of 120° in three-phase operation means that the total current is always zero like Fig. 4, as a result of which L_{mbi} create no effective magnetic fluxes. Thus, L_{mbi} does not affect how L_{mj}, L_{ri}, and C_{ri} resonate.

The diode denoted by D_r in Fig. 3 returns the output power into the input, and thereby the input power source supplies only the electricity equivalent to the power loss of the system, leading to the precise measurement of power conversion efficiency [33].

In this configuration, V_o and V_{in} are almost identical and thus the *gain* defined as V_o/V_{in}, described in Section III-D, is approximately 1. For gain = 1, output power can be adjusted by switching frequency (f_{sw}) according to the *gain* equation of *LLC* that takes secondary leakage inductance and resistance components into account as mentioned in Section III-D. The authors adjusted f_{sw} of Q_j to obtain the expected output power.

B. Transformer Design

The following restraints should be simultaneously taken into account to design transformers that are as small as possible.

1) The transformers must always work below their saturation magnetic flux density.
2) The maximum magnetic flux density during operation must be reduced in order to minimize core losses P_{core}.
3) Primary winding number (N_p) and secondary winding number (N_s) and the actual area of the core (A_e) should be small in order to downsize the power supply unit.

Less magnetic flux density during operation is crucial for an appropriate transformer design because the density directly determines how large P_{core} is. The maximum magnetic flux density B_m at duty = 0.5 is generally expressed as [34]

$$B_m = \frac{V_{\text{in}}}{8 f_{\text{sw}} N_p A_e} (\text{T}). \tag{1}$$

The equation elucidates that we have to increase at least one of f_{sw}, N_p, or A_e in order to reduce B_m under a constant V_{in}. Larger N_p or A_e, however, leads to larger transformers and thus these options conflicts with the demands to miniaturize power supplies. Therefore, the only measure we take is to increase f_{sw}, and SiC MOSFETs can meet this demand. The authors set f_{sw} around 200 kHz, which Si IGBTs cannot reach. The team chose the transformer core material, power ferrites PC40 (TDK), due to its high resistivity and its consequent low eddy current losses suitable for high f_{sw} [35]. The saturation flux density B_s is 380 mT for PC40 at 100 °C, and thus 150 mT was adopted for the B_m in order to reduce P_{core} at 200 kHz and to avoid reaching the B_s. PC40EER28L-Z(TDK) is selected as a core component suited with our purpose, and its effective core volume V_e is 6.15 cm^3.

The design parameters for the transformers are summarized as follows:

1) $V_{\text{in}} = 600\,\text{V}$;
2) $V_o = 600\,\text{V}$;
3) Maximum $B_m = 150\,\text{mT}$;
4) $f_{\text{sw}} = 200\,\text{kHz}$;
5) $A_e = 0.814\,\text{cm}^2$.

These values and (1) dictate N_p to be 30.71 turns. The team used two series transformers as an isolation transformer in order to spread heat and specify N_p to be 16. Since N_s/N_p is to be equal to $V_{\text{o}}/V_{\text{in}}$, N_s must be 16. The value of C_{ri} is chosen to be less than 100 nF to keep the capacitor size small. For this, an L_{ri} value greater than 6μH is sufficient if we set f_{sw} to be around 200 kHz. After winding the transformers, we measured the L_r value to be about 12 μH. Hence, a necessary value of C_r was approximately 60 nF to create a resonance f_{sw} of 200 kHz. S, defined as L_r/L_m, is set to be 0.1 for the same practical reasons as described in [36]. Thus, the authors adopted the two-series L_{mj} values to be about 120 μH. L_{mbi} value should be large enough to compensate for the three-phase deviations of each resonant parameter (C_{ri} and L_{ri}). Therefore, we chose L_{mbi} value to be about twice as large as L_{ri} value to balance each phase current.

TABLE I
LLC CIRCUIT PARAMETERS

Input voltage (V_{in})	600 V
Input capacitances (C_{in1},C_{in2})	2200 μF
Switches (Q_j, j = 1–6)	SiC MOSFET (SCT2080KE) Rohm (BV = 1200 V, R_{on} = 80 mΩ)
Magnetic inductances (L_{mj}, j = 1 – 6)	55.6, 55.1, 64.3, 51.8, 56.2, and 57.5 μH
Resonant inductances (L_{ri}, i = 1 – 3)	12.0, 11.6, and 11.6 μH
Magnetic inductances of the balanced transformer (L_{mbi}, i = 1 – 3)	20.7, 21.0, and 19.7 μH
Resonant capacitances (C_{ri}, i = 1 – 3)	60 nF
Secondary diodes (D_{oj}, j = 1 – 6)	SiC SBD (SCS210KG) Rohm (BV = 1200 V)
Regenerating diode (D_r)	SiC SBD (SCS210KG) Rohm (BV = 1200 V)
Output capacitances (C_{o1}, C_{o2})	270 μF
Output Voltage (V_o)	600 V

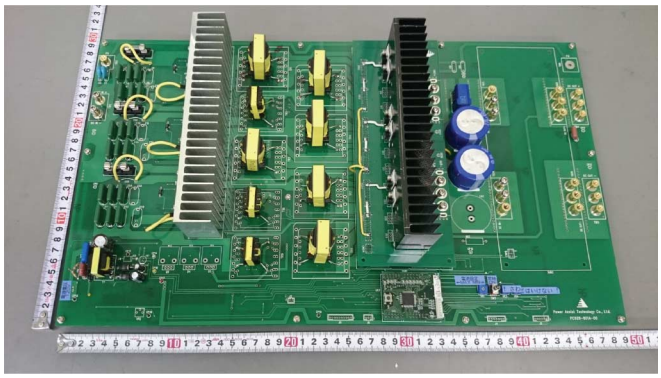

Fig. 5. Picture of the prototype 5-kW three-phase *LLC* series resonant dc/dc measuring 49-cm wide and 29-cm long.

Si IGBTs have been shown to operate at up to 50 kHz [37]. A f_{sw} of 50 kHz would result in transformers with A_e and V_e of 3.44 and 35.1 cm^3, respectively, when using the same core material (PC40EE57/47-Z) N_p and N_s as presented above. In this case, 200-kHz switching frequency reduces V_e by 82%.

C. System Configuration

All the circuit constants used in our *LLC* dc/dc are listed in Table I. Fig. 5 presents the picture of the *LLC* dc/dc circuit board used in the experiments implemented here and two rulers are also added in the figure providing a guide for the size of the *LLC* dc/dc.

The following discussions are based on the circuit in Fig. 3.

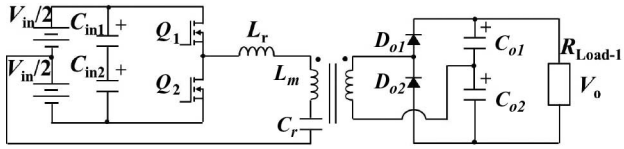

Fig. 6. Single-phase leg circuit of the three-phase *LLC* dc/dc shown in Fig. 3.

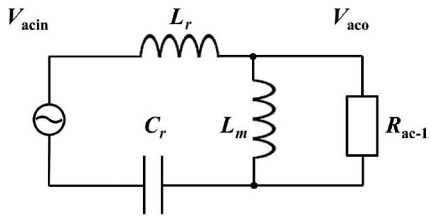

Fig. 7. Equivalent circuit of Fig. 6 simplified by FHA.

D. Gain Analysis Model of the LLC

Fig. 6 exhibits a single-phase circuit equivalent to the three-phase *LLC* dc/dc in Fig. 3, and here $R_{\text{Load-1}}$ is the load resistance in the equivalent single-phase circuit.

The *LLC* circuit utilizes the resonance among L_r, L_m, and C_r, and consequently the current flowing in the circuit has a nearly sinusoidal waveform, which validates the use of first harmonic approximation (FHA) as a measure to analyze how the circuit behaves [38]. The simplified circuit is first considered equipped with a simple ac input shown in Fig. 7 in order to obtain the mathematical expression of the total load corresponding to $R_{\text{Load-1}}$ in FHA, $R_{\text{ac-1}}$. In FHA, V_{acin} and V_{aco} can be expressed as

$$V_{\text{acin}} = \frac{2}{\pi} V_{\text{in}} \sin(2\pi f_{\text{sw}} t)$$
$$V_{\text{aco}} = \frac{2}{\pi} V_{\text{o}} \sin(2\pi f_{\text{sw}} t).$$

In this case, the output power $P_{\text{out-1}}$ can be expressed as

$$P_{\text{out-1}} = \frac{V_o^2}{R_{\text{Load-1}}} = \frac{V_{\text{aco,rms}}^2}{R_{\text{ac-1}}} = \frac{\left(\frac{2V_{\text{o}}}{\sqrt{2}\pi}\right)^2}{R_{\text{ac-1}}}$$

where the subscription of "rms" denotes effective value. Thus, $R_{\text{ac-1}}$ is equal to

$$R_{\text{ac-1}} = \frac{2}{\pi^2} R_{\text{Load-1}}. \quad (2)$$

The circuit in Fig. 7, however, is too simple to analyze the *LLC* dc–dc circuit. L_r should be divided into primary leakage inductance L_{lkp} and secondary leakage inductance L_{lks} to improve the accuracy of circuit simulation [39]. In addition, resistive components should be taken into account for improving the quality of analysis; the components include R_{ON} of transistors, forward resistance of diodes (R_D), and wire resistance R_{w1} and R_{w2} of primary and secondary transformers. Thereby, we modify the circuit model in [39], and analyze the *LLC* circuit performance based on the circuit shown in Fig. 8, where $R_P = R_{\text{ON}} + R_{w1}$, and $R_S = R_D + R_{w2}$.

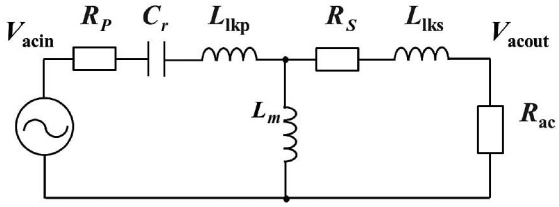

Fig. 8. Equivalent circuit of Fig. 6 simplified by FHA considering L_{lkp}, L_{lks}, R_D, R_{ON}, R_{w1}, and R_{w2}.

Assuming that $L_{lkp} = L_{lks}$, the *gain* (M_{-1}) is calculated by

$$M_{-1} \equiv \frac{V_o}{V_{in}} = \frac{V_{aco,rms}}{V_{acin,rms}} = \left| \frac{L_m R_{ac\text{-}1}}{jX_{-1} + Y_{-1}} \right| \tag{3}$$

where

$$X_{-1} = 2\pi f_{sw} L_{lkp}(L_p + L_m) - \frac{1}{2\pi f_{sw}} \left(R_P R_{A-1} + \frac{L_p}{C_r} \right)$$
$$Y_{-1} = L_p(R_P + R_{A-1}) - \frac{1}{4(\pi f_{sw})^2} \frac{R_{A-1}}{C_r}$$
$$R_{A-1} \equiv R_S + R_{ac-1}, \quad L_p \equiv L_m + L_{lkp}.$$

The three-phase *LLC* resonant converter corresponds to three parallel connected circuits of Fig. 8, and the load resistance of the three-phase *LLC* $R_{ac\text{-}3}$ is equal to 1/3 of $R_{ac\text{-}1}$. Thus, (3) can be used to express the *gain* for the three-phase *LLC* M_{-3} as follows:

$$M_{-3} = \left| \frac{L_m R_{ac\text{-}3}}{jX + Y} \right| \tag{4}$$

where

$$R_{A-3} = R_S + R_{ac\text{-}3}$$
$$X_{-3} = 2\pi f_{sw} L_{lkp}(L_p + L_m) - \frac{1}{2\pi f_{sw}} \left(R_P R_{A-3} + \frac{L_p}{C_r} \right)$$
$$Y_{-3} = L_p(R_P + R_{A-3}) - \frac{1}{4(\pi f_{sw})^2} \frac{R_{A-3}}{C_r}.$$

The mathematical model in [39], and (4) discussed above are applied to obtain the gain characteristics of the three-phase *LLC* dc/dc. Fig. 9(a) and (b) presents the *gain* curves as a function of f_o/f_{sw}, where f_o denotes the *LLC* resonance frequency as defined by

$$f_o = \frac{1}{2\pi\sqrt{(L_{lkp} + L_{lks})C_r}}. \tag{5}$$

The curves in Fig. 9(a) are based on the model in [39]; the ones in Fig. 9(b) are obtained by use of (4) and each resistance parameter corresponding to its output condition (e.g., $R_p = 0.26\ \Omega$, $R_s = 1.22\ \Omega$ at 5-kW output power). These two part figures also include the experimental results as denoted by solid black circles, which results come from the f_{sw}-output power correlation presented in Fig. 9(c) as denoted by the solid blue line and the open blue circle markers.

As clearly shown in Fig. 9(a) and (b), our analytical model provides an improvement on the model in [39] and coincides closely with the experimental results. Therefore, these

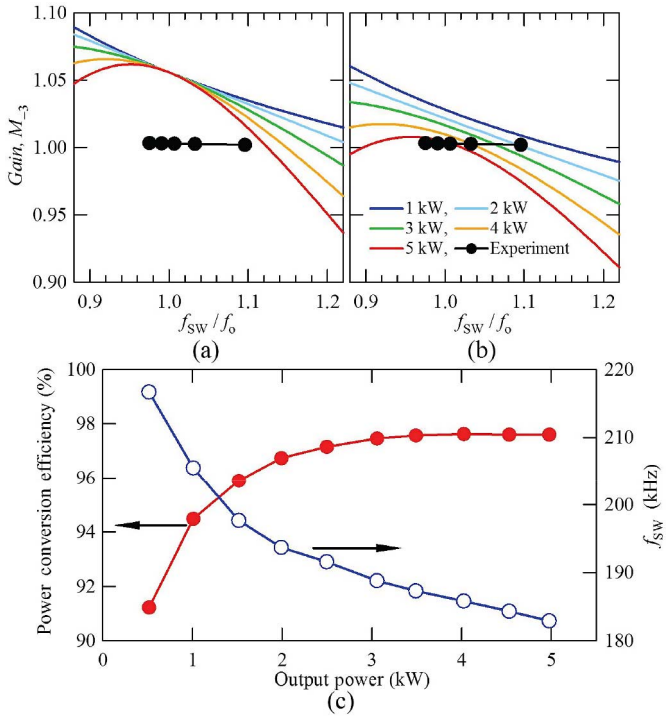

Fig. 9. Calculated *gain* of M_{-3} [(a) and (b)] and the experimental *Gain* results [solid black circles in (a) and (b)] as a function of f_o/f_{sw}. (a) is for the case of no contributions from resistive components, and the curves in (b) are obtained by use of (4). (c) Experimental results of how power conversion efficiency and f_{sw} depend on the output power of the *LLC* dc–dc.

experiment data validate our model including the contribution of resistive components in *LLC* resonant tank. This also indicates that the resistive components play an important role to determine the gain – f_{sw} characteristics of *LLC*.

Fig. 9(c) also includes power conversion efficiency at various output powers of our *LLC* dc/dc. The power conversion efficiency was estimated by the use of the amount of energy the input power source supplied during operation, because the amount is regarded as the power loss of the *LLC* as described in SectionIII-A. The best measured power efficiency of our *LLC* dc/dc achieves 97.6% at 5-kW. Applied f_{sw} can reach around 200 kHz owing to the high speed switching characteristic of SiC MOSFETs. The output power varied with f_{sw} through the mechanism as explained in this section.

IV. Experimental Results

A. Switching Waveforms

Fig. 10 shows the measured waveforms of drain-source voltage V_{ds} and drain current I_d of SiC MOSFET Q_1. The use of SiC MOSFETs enables high f_{sw} (200 kHz) driving and high V_{in} (600 V). This figure also indicates very small crossing area of V_{ds} and I_d curves, meaning that soft switching works well in this circuit configuration.

B. Effects of Balanced Transformer Circuit

How the balanced transformers worked is displayed in Fig. 11(a) and (b). The waveforms in this figure represent each

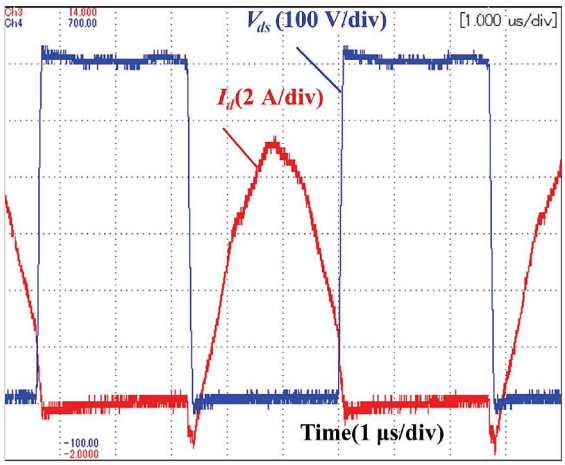

Fig. 10. Waveforms of V_{ds} and I_d of Q_1.

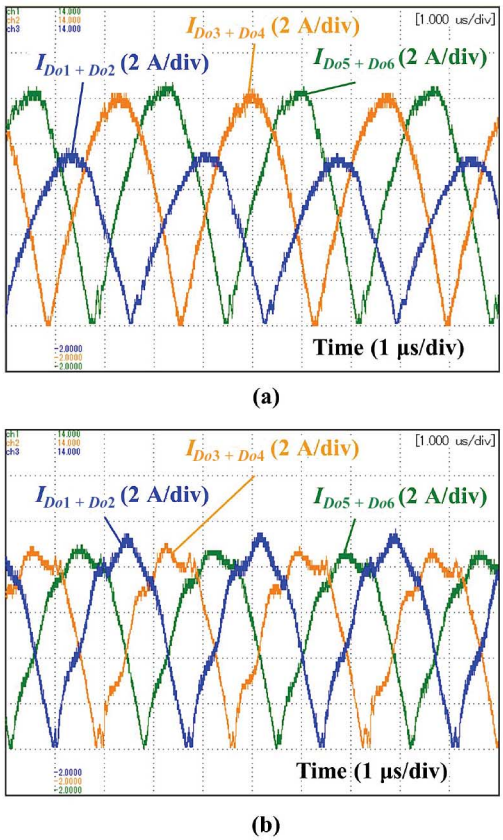

Fig. 11. Waveforms of current flowing through $D_{o1} + D_{o2}$ ($I_{Do1+Do2}$), $D_{o3} + D_{o4}$ ($I_{Do3+Do4}$), and $D_{o5} + D_{o6}$ ($I_{Do5+Do6}$) with (a) no balanced transformers and (b) with balanced transformers.

current per phase flowing through a serially connected pair of secondary diodes in each single-phase secondary circuit. The *LLC* circuit without balanced transformers fails in equalizing current per phase, and the sum of all the individual phase currents has a maximum peak-to-peak value (ΔI_{ripple}) is 6.45 A as shown in Fig. 11(a). The *LLC* circuit with balanced transformers, the whole design of which displays in Fig. 3, decreases the ΔI_{ripple} to about 4.31 A.

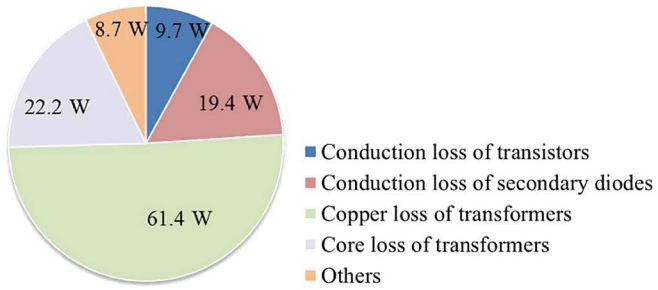

Fig. 12. Loss breakdown pie chart.

Reducing ΔI_{ripple} leads to downsized C_{in} and C_o in Fig. 3. The minimum value for the input or output capacitance C_m must satisfy [40]

$$C_m = \frac{\Delta I_{\text{ripple}} \times T_{\text{ON}}}{\Delta V_{\text{ripple}}} \tag{6}$$

where ΔV_{ripple} denotes the maximum difference between peak voltages, and T_{ON} for on-time of switch Q_i. Equation (6) proves that less ΔI_{ripple} leads to less C_m.

In the case where ΔV_{ripple} is 0.6 V, corresponding to 0.1% of V_{in} 600 V, C_m is 29.5 μF for an unbalanced circuit. On the other hand, with a balanced circuit condition, 19.7 μF is enough for C_m, meaning that the balanced circuit is capable of reducing the capacitor size.

In addition, small ΔI_{ripple} enables *LC* filters to be removed from the circuit. An *LC* filter delays current and causes worse response for the feedback component. This current-balanced circuit reported here operates more effectively even in a high output current system.

C. Loss Analysis

The pie chart of Fig. 12 shows the loss breakdown of the SiC-based *LLC* dc–dc at 5-kW output power. The effective value of current through the transistors was 4.5 A. The SiC MOSFETs used here has an R_{ON} of 80 mΩ and thus, the total conduction loss of the transistors was $(4.5\,\text{A})^2 \times 80\,\text{m}\Omega \times 6\,\text{pcs} = 9.7\,\text{W}$. For the secondary diodes, the average absolute current was observed to be 2.94 A. The forward voltage at 2.94 A was 1.1 V, and accordingly the total loss at the secondary diodes was $2.94\,\text{A} \times 1.1\,\text{V} \times 6\,\text{pcs} = 19.4\,\text{W}$.

The total resistance of the transformer winding copper used here was 1.66 Ω at 183 kHz. The effective value of the current through the transformers is 6.08 A, and thus the copper loss of the transformers was $(6.08\,\text{A})^2 \times 1.66\,\Omega = 61.4\,\text{W}$. Another major loss factor in the transformers, core loss, was calculated as follows. Equation (1) provides a B_m of 0.157 T by using $A_e = 0.814\,\text{cm}^3$, $N_p = 16$ turn, $f_{\text{sw}} = 182.9\,\text{kHz}$, and an input voltage for each transformer of 300 V. This B_m generates a core loss of 22.2 W according to the B_m-core loss correlation in the datasheet of PC40EER28L-Z.

A difference between the total loss and the sum of these aforementioned losses still remains and, accordingly, the difference is denoted by "others" in Fig. 12. These losses mainly comprise the switching loss of the SiC MOSFETs, and the core loss in the balanced transformers.

V. Conclusion

This paper has reported on a three-phase 5-kW *LLC* dc/dc converter comprising SiC MOSFETs with 1200-V *BV* as switching devices to prove the advantages of SiC devices. Around 200 kHz switching, a frequency SiC MOSFETs can reach but Si IGBTs cannot, successfully reduces the volume of the isolation transformers. The high *BV* of SiC MOSFETs, enables a V_{in} up to 600 V and also has the potential to raise V_{in} over 800 V. Thus we will experiment with 800 V input *LLC* dc/dc equipped SiC MOSFETs to verify the potential in the next phase of the research. A three-phase configuration allows decreased currents, as a result of which the *LLC* dc/dc maintains good enough power conversion efficiency avoiding the rise of switching loss caused by high f_{sw}. The additional transformers to balance three-phase currents suppress a peak current in the circuit, minimizing C_{in} and C_o to absorb current ripples in the circuit.

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