Grid-Connected Boost-Half-Bridge Photovoltaic Micro Inverter System Using Repetitive Current Control and Maximum Power Point Tracking

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Abstract*— This paper presents a novel boost-half-bridge micro inverter and its control implementations for single-phase grid-connected photovoltaic systems. The proposed topology consists of a transformer isolated boost-half-bridge DC-DC converter and a full-bridge pulse-width-modulated inverter. The boost-half-bridge converter integrates the conventional boost converter and the half-bridge converter by using only two active devices. The promising features such as circuit simplicity, low cost, high efficiency and high reliability are obtained. Moreover, a high performance plug-in repetitive controller is proposed to regulate the grid current. High power factor (> 0.99) and very low total harmonic distortions (0.9% ~ 2.87%) are guaranteed under both heavy and light load conditions. Dynamic stiffness is also achieved under load step change conditions. In addition, a variable step size MPPT method is adopted such that fast tracking speed and high MPPT efficiency are both guaranteed. A 210W prototype was fabricated and tested. Simulation and experimental results are provided to verify the validity and performance of the circuit operations, current control and MPPT algorithm.

I. INTRODUCTION

The concept of micro inverter (also known as module integrated converter/inverter) has become a future trend for single-phase grid-connected photovoltaic power systems, for its removal of energy yield mismatches among PV modules, possibility of individual PV module oriented optimal design, independent maximum power point tracking (MPPT), and "plug and play" concept [1], [2]. In general, a micro inverter system is often supplied by a low voltage solar panel, which requires a high voltage step-up ratio to produce desired output AC voltage [1]-[3]. Hence, a DC-DC converter cascaded by an inverter is the most popular topology, in which a high frequency transformer is often implemented within the DC-DC conversion stage [4]-[10].

In terms of the pulse-width modulation (PWM) techniques employed by the micro inverter system, two major categories are attracting most of the attentions. In the first, PWM control is applied to both of the DC-DC converter and the inverter [4]-[6]. In addition, a constant voltage DC link decouples the power flow in the two stages such that the DC input is not affected by the double-line-frequency power ripple appearing at the AC side. By contrast, the second configuration utilizes a quasi-sinusoidal PWM method to control the DC-DC converter in order to generate a rectified sinusoidal current (or voltage) at the inverter DC link. Accordingly, a line-frequency commutated inverter unfolds the DC link current (or voltage) to obtain the sinusoidal form synchronized with the grid [7]-[10]. Although the latter has the advantage of higher conversion efficiency due to the elimination of high frequency switching losses at the inverter, the double-line-frequency power ripple must be all absorbed by the DC input capacitor, making the MPPT efficiency compromised unless a very large capacitance is used. Moreover, the DC-DC conversion stage requires more challenging control techniques to meet the grid current regulation requirement. Therefore, in terms of the MPPT performance and output current quality, the first category of micro inverter is more appropriate and will be adopted in this paper.

A boost dual-half-bridge DC-DC converter for bidirectional renewable energy conversion applications was first proposed by [11] and then further investigated in [12]-[14]. It integrates the boost converter and the dual-half-bridge converter together by using minimal number of devices. High efficiency is realizable when the zero voltage switching (ZVS) technique is adopted. By replacing the secondary half bridge with a diode voltage doubler, a new boost-half-bridge converter can be derived for unidirectional power conversions [15]. In this paper, the boost-half-bridge converter is incorporated as the DC-DC conversion stage for the grid-connected photovoltaic micro inverter system. Simplicity of the circuit structure, ease of control, and minimal number of semiconductor devices exhibit promising features such as low cost, high efficiency and high reliability.

A full-bridge PWM inverter with an output LCL filter is incorporated to inject synchronized sinusoidal current to the grid. In general, it is desirable to have low total harmonic distortions (THD) of the grid current and close-to-unity power factor under general load conditions and non-ideal grid voltages. Repetitive control (RC) is known as an effective solution for elimination of periodic harmonic errors and has been previously investigated and validated in the UPS systems [16]-[20], active power filters [21], [22], and PWM rectifiers [23]. In [20], a linear phase infinite

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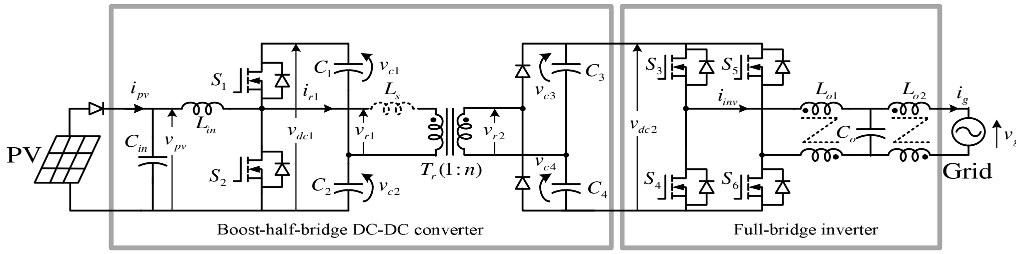

Fig. 1. Proposed boost-half-bridge micro inverter for grid-connected photovoltaic systems

impulse response (IIR) filter has been synthesized for the RC based UPS systems. This IIR filter is implemented to obtain very high system open loop gains at a large number of harmonic frequencies such that the harmonic rejection capability is greatly enhanced. In this paper, a plug-in repetitive current regulator is proposed based on the IIR filter in [20]. It consists of a proportional part which guarantees fast dynamics, and an RC part which is dedicated to the rejection of steady state harmonic distortions.

MPPT is performed by the boost-half-bridge DC-DC converter. Numerous MPPT techniques have been studied and verified, for example, perturb & observe (P & O) method [26]-[29], incremental conductance method [30], ripple correlation method [31], reduced current sensor method [32], etc. Different techniques have shown different trade-offs among the steady state MPPT efficiency, the transient tracking speed, and the control complexity [33], [34]. Variable step size P & O method is an improvement from the most popular P & O method. It modifies the tracking steps adaptively in order to achieve fast convergence and high MPP regulation accuracy simultaneously. In this paper, an MPPT method where the P-V curve is divided into three different operation zones, each of which uses a different step size, is developed. The adopted MPPT algorithm is able to approach the MPP fast and oscillates with a very small ripple around the MPP.

II. BOOST-HALF-BRIDGE MICRO INVERTER

The proposed boost-half-bridge micro inverter topology for grid-connected photovoltaic systems is depicted in Fig. 1. It is composed of two decoupled power processing stages. In the front-end DC-DC converter, a conventional boost converter is modified by splitting the output DC capacitor into two separate ones. C_{in} and L_{in} denote the input capacitor and boost inductor, respectively. The center taps of the two MOSFETs (S_1 and S_2) and the two output capacitors (C_1 and C_2) are connected to the primary terminals of the transformer T_r, just similar to a half-bridge. L_s represents the transformer leakage inductance reflected to the primary and $1:n$ is the transformer turns ratio. A voltage doubler composed of two diodes (D_1 and D_2) and two capacitors (C_3 and C_4) is incorporated to rectify the transformer secondary voltage to the inverter DC link. A full-bridge inverter composed of 4 MOSFETs (S_3 ~ S_6) using SPWM control serves as the DC-AC conversion stage. Sinusoidal current with a unity power factor is supplied to the grid through a third-order LCL filter (L_{o1}, L_{o2} and C_o).

Other symbol representations are defined as follows. d_1 denotes the duty cycle of S_1 and T_{sw1} is the switching period of the boost-half-bridge converter. i_{pv} and v_{pv} represent the PV current and voltage, respectively. The voltages across C_1, C_2, C_3 and C_4 are denoted by v_{c1}, v_{c2}, v_{c3} and v_{c4}, respectively. v_{r1}, v_{r2} and i_{r1} stand for the transformer primary voltage, secondary voltage and primary current, respectively. v_{dc1} is the low voltage side (LVS) DC link voltage and v_{dc2} is the high voltage side (HVS) DC link voltage. T_{sw2} is the switching period of the full bridge inverter. i_{inv} and i_g are the output AC current at the inverter side and the grid side, respectively. v_g is the grid voltage.

The boost-half-bridge converter is controlled by S_1 and S_2 with complementary duty cycles. Neglect all the switching dead bands for simplification. The idealized transformer operating waveforms are illustrated in Fig. 2. When S_1 is on and S_2 is off, v_{r1} equals to v_{c1}. When S_1 is off and S_2 is on, v_{r1} equals to $-v_{c2}$. At the steady state, the transformer volt-sec is always automatically balanced. In other words, the primary volt-sec A_1 (positive section) and A_2 (negative section) are equal. So are the secondary volt-sec A_3 (positive section) and A_4 (negative section). Normally, D_1 and D_2 are on and off in a similar manner as S_1 and S_2, but with a phase delay t_{pd} due to the transformer leakage inductance. Ideally, the transformer current waveform is determined by the relationships of $v_{c1} \sim v_{c4}$, the leakage inductance L_s, the phase delay t_{pd}, and S_1's turn-on time $d_1 T_{sw1}$.

For simplicity, hard switching is employed and the transformer leakage inductance is regarded as small enough in this paper. Therefore, Eq. (1) and (2) can be derived as follows.

$$v_{c1} = \frac{(1-d_1)}{d_1} v_{pv},\ v_{c2} = v_{pv},\ v_{dc1} = \frac{v_{pv}}{d_1} \tag{1}$$

$$v_{c1} = \frac{(1-d_1)}{d_1} v_{pv},\ v_{c2} = v_{pv},\ v_{dc1} = \frac{v_{pv}}{d_1} \tag{2}$$

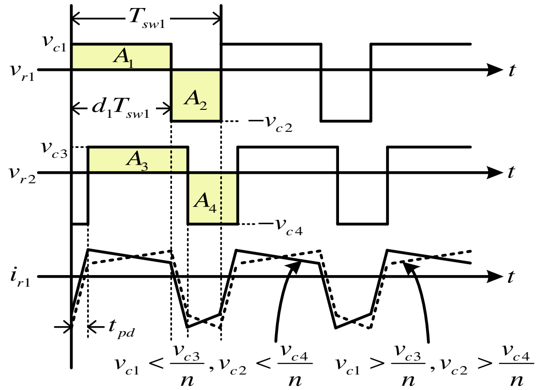

Fig. 2. Idealized transformer voltage and current

III. REPETITIVE CONTROLLER DESIGN

An all digital approach is adopted for the control of the proposed boost-half-bridge micro inverter as Fig. 3 shows. v_{pv} and i_{pv} are both sensed for calculation of the instantaneous PV power P_{pv} , the PV power variation ΔP_{pv} , and the PV voltage variation Δv_{pv} . ΔP_{pv} and Δv_{pv} are utilized for the MPPT purpose. The MPPT function block then generates a reference v_{pv}^* for the inner loop of the PV voltage regulation, which is performed by the DC-DC converter. At the inverter side, the grid voltage v_g is sensed to extract the instantaneous sinusoidal angle θ_g, which is commonly known as the phase lock loop (PLL). The inverter output current i_{inv} is pre-filtered by a first-order low pass filter on the sensing circuitry for elimination of high frequency noises. The filter output i_{inv}' is then fed back to the plug-in repetitive controller for regulation as the inner loop. Either v_{dc1} or v_{dc2} can be sensed for the DC link voltage regulation as the outer loop. In practice, the LVS DC link voltage v_{dc1} is regulated for cost effectiveness. i_{inv}^* and v_{dc1}^* represent the grid current reference and the LVS DC link voltage reference, respectively.

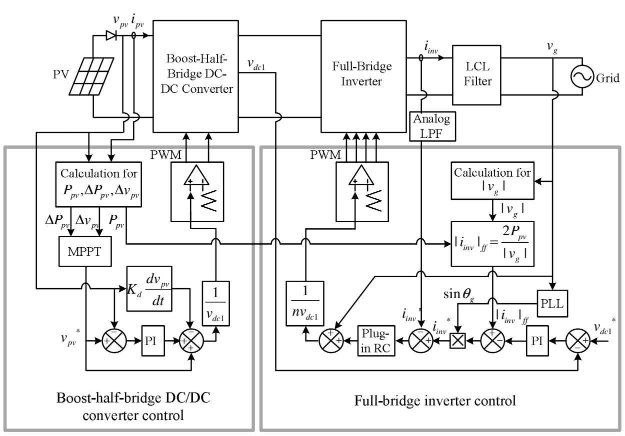

Fig.3. Architecture of the proposed micro inverter system control

In order to achieve fast dynamic responses of the regulations of the grid current as well as the DC link voltage, a current reference feed forward is added in correspondence to the input PV power P_{pv} . The magnitude of the current feed forward is expressed as

$$\left|i_{inv}\right|_{ff} = \frac{2P_{pv}}{\left|v_g\right|} \tag{3}$$

where $\left|v_g\right|$ is the magnitude of the grid voltage and can be calculated by

$$\left|v_g\right| = \frac{1}{2}\int_0^{\pi} v_g d\theta_g \tag{4}$$

IV. PLUG-IN REPETITIVE CONTROLLER

In this paper, the LCL parameters are selected by following the guidelines provided in [35] and [38]. The current sensor is placed at the inverter side. TABLE I summarizes the key parameters of the full-bridge inverter.

TABLE I
FULL-BRIDGE INVERTER PARAMETERS

HVS DC link voltage	370V
Switching frequency	10.8kHz
Sampling frequency	10.8kHz
Rated output power	210W
Grid voltage	180V ~ 240V
Grid line frequency	60Hz
Filter inductor (L_{o1}, L_{o2})	8.5mH
Filter capacitor (C_o)	330nF

A. Plant Transfer Function

The control-output-to-inverter-current transfer function in the continuous time domain can be derived as

$$G_{LCL}(s) = \frac{(L_{o2}C_o s^2 + r_2 C_o s + 1)e^{-sT_d}}{L_{o1}L_{o2}Cs^3 + (r_1 L_{o2} + r_2 L_{o1})C_o s^2 + (r_1 r_2 C_o + L_{o1} + L_{o2})s + r_1 + r_2} \tag{5}$$

where r_1 and r_2 represent the equivalent series resistance of L_{o1} and L_{o2}, respectively. Based on the power loss estimation of the inductors, $r_1 = 1.4\Omega$ and $r_2 = 1.0\Omega$. From (5), the LC resonance frequency is

$$\omega_r = \sqrt{\frac{r_1 r_2 C_o + L_{o1} + L_{o2}}{L_{o1}L_{o2}C_o}} \tag{6}$$

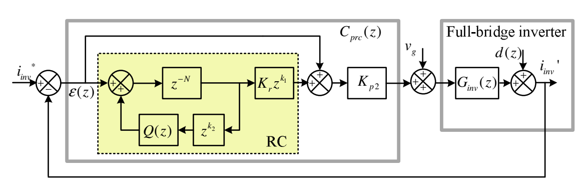

Fig.4. Block diagram of the proposed plug-in repetitive controller

The system hardware and software delay is summarized as T_d, which is typically around one and a half sampling period ($T_d = 140\mu s$). In order to reduce the switching noises in the sensed inverter current, an analog low pass filter (7) is placed on the current feedback path.

$$F_{LPF}(s) = \frac{\omega_{fc}}{s + \omega_{fc}} \tag{7}$$

The cut-off frequency is chosen as $\omega_{fc} = 4\times10^4\, rad/s$. Therefore, by using the zero-order hold discretization scheme, the entire plant combining (5) and (7) can be discretized as

$$G_{inv}(z) = \frac{0.00265z^{-2} + 0.00548z^{-3} + 0.00474z^{-4} + 0.00559z^{-5} + 0.000254z^{-6}}{1 + 0.5468z^{-1} - 0.5653z^{-2} - 0.9606z^{-3} + 0.024z^{-4}} \tag{8}$$

B. Plug-in Repetitive Control Scheme

The plug-in digital repetitive controller is designed as Fig. 4 shows. The conventional proportional controller with a gain of K_{p2} is incorporated to guarantee fast dynamics. The RC is then plugged into the system and operates in parallel with the proportional controller.

$\varepsilon(z)$ and $d(z)$ represent the tracking error and the repetitive disturbances, respectively.

The modified internal model [24], which is denoted by the positive feedback loop inside the RC, plays the most critical role in the proposed current regulator. z^{-N} is the time delay unit where N denotes the number of samples in one fundamental period. In an ideal RC, a unity gain is along the positive feedback path such that all the repetitive errors based on the fundamental period are completely eliminated when the system reaches equilibrium. However, in order to obtain a sufficient stability margin, a zero-phase low pass filter is often incorporated rather than the unity gain. This can be realized by cascading a linear phase low pass filter $Q(z)$ and a non-causal phase lead compensator z^{k_2}. z^{k_1} is another non-causal phase lead unit which compensates the phase lag of $G_{inv}(z)$, particularly at high frequencies. Here k_1 and k_2 both stand for the number of sampling periods. K_r is the constant gain unit that determines the weight of the RC in the whole control system.

From Fig. 4, the transfer function of the entire plug-in RC current regulator can be described as

$$C_{prc}(z) = \frac{K_r K_{p2} z^{-N} z^{k_1}}{1 - Q(z) z^{k_2} z^{-N}} + K_{p2} \tag{9}$$

C. Analysis and Design of the Plug-in RC

The selection of K_{p2} follows exactly the same rules as the conventional proportional controller design. Basically, it requires a trade-off between the obtainable stability margin and the current regulation performance. In this paper, $K_{p2} = 50$ is selected.

From Fig. 4, the tracking error $\varepsilon(z)$ can be derived as

$$\begin{aligned} \varepsilon(z) &= \varepsilon(z) z^{-N}\left[Q(z) z^{k_2} - \frac{K_r K_{p2} z^{k_1} G_{inv}(z)}{1 + K_{p2} G_{inv}(z)}\right] \\ &+ \left[\frac{1 - Q(z) z^{k_2} z^{-N}}{1 + K_{p2} G_{inv}(z)}\right]\left[i_{inv}^{\ *}(z) - d(z)\right] \end{aligned} \tag{10}$$

It is noticeable that a larger K_{p2} will result in a smaller tracking error during the transient because the second summation term on the right side of (10) is reduced. This exactly explains the function of the proportional control part.

Let $\left|H(z)\right|_{z=e^{j\omega T_{sw2}}} = \left|Q(z) z^{k_2} - \frac{K_r K_{p2} z^{k_1} G_{inv}(z)}{1 + K_{p2} G_{inv}(z)}\right|$, $\omega \in [0, \frac{\pi}{T_{sw2}}]$, in which T_{sw2} is also the sampling period. A sufficient condition for the system stability is

$$\left|H(e^{j\omega T_{sw2}})\right| < 1 \tag{11}$$

With further manipulation on (10), the steady state error can be derived as

$$\left|\varepsilon(z)\right| = \left|i_{inv}^{\ *}(z) - d(z)\right| \left|\frac{1 - Q(z) z^{k_2}}{\left[1 + K_{p2} G_{inv}(z)\right]\left[1 - H(z)\right]}\right| \tag{12}$$

From (11) and (12), the general design criteria of $Q(z)$ for obtaining a good stability as well as a small steady state error can be summarized as: 1) $Q(z)$ must have sufficient attenuation at high frequencies; 2) $Q(z)$ must be close to unity in a frequency range which covers a large number of harmonics; 3) $Q(z) z^{k_2}$ must have a zero phase when $Q(z)$ is close to unity.

In [20], a 4^{th}-order linear phase IIR filter is synthesized for the repetitive voltage controller for UPS systems. Compared with the conventional linear phase finite impulse response (FIR) filters used for the repetitive control, the linear phase IIR filter exhibits a flat gain in the pass band and a much faster roll off in the transition band, when the filter order is given [20], [25]. Hence, it is a good candidate for the repetitive current controller in this paper as well.

In practice, $Q(z)$ is synthesized by cascading a 2^{nd}-order elliptic filter $Q_e(z)$ and a 2^{nd}-order all-pass phase equalizer $Q_a(z)$. $Q(z)$, $Q_e(z)$ and $Q_a(z)$ are expressed by (13)-(15).

$$Q(z) = Q_e(z) Q_a(z) \tag{13}$$

$$Q_e(z) = \frac{0.1385 + 0.2564z^{-1} + 0.1385z^{-2}}{1 - 0.7599z^{-1} + 0.2971z^{-2}} \tag{14}$$

$$Q_a(z) = \frac{0.1019 - 0.6151z^{-1} + z^{-2}}{1 - 0.6151z^{-1} + 0.1019z^{-2}} \tag{15}$$

The bode plots of $Q_e(z)$, $Q_a(z)$ and $Q(z)$ are shown in Fig. 5. The linear phase region of $Q(z)$ is from 0 to 1403 Hz (8816 rad/s). $k_2 = 5$ is selected to compensate the phase delay of $Q(z)$ to zero. The maximum pass band gain and the cut-off frequency of $Q(z)$ is 0.9975 and 1670 Hz, respectively.

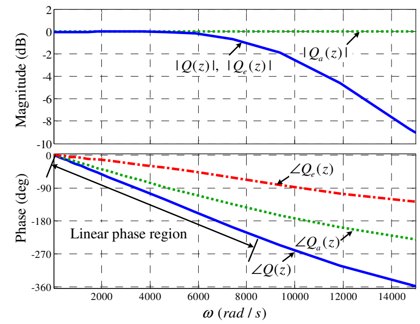

Fig. 5. Bode plots of $Q_e(z)$, $Q_a(z)$ and $Q(z)$

The locus of $H(e^{j\omega T_{sw2}})$ is useful for guiding the selection of K_r and k_1. The fundamental principle for choosing K_r and k_1 is that $H(e^{j\omega T_{sw2}})$ should keep a sufficient margin from the unity circle when ω increases from 0 to the nyquist frequency π/T_{sw2}. When K_r and k_1 are assigned with different values, $H(e^{j\omega T_{sw2}})$ can be plotted in Fig. 6(a) and (b). In Fig. 6(a), K_r is fixed, $k_1 = 4$ renders a good stability margin. Likewise, $K_r = 0.3$ would be an appropriate choice from Fig. 6(b).

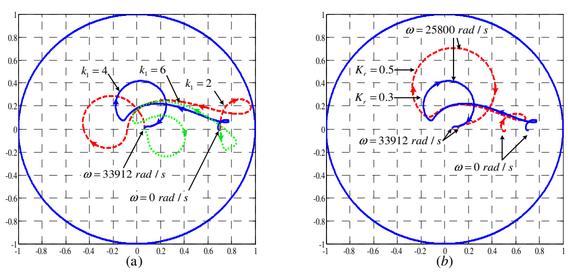

Fig. 6. Locus of the vector $H(e^{j\omega T_{sw2}})$. (a) $K_r = 0.3$, k_1 is varying; (b) $k_1 = 4$, K_r is varying.

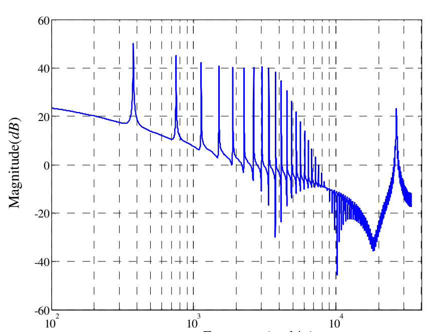

Fig. 7. Frequency response of $|C_{prc}(z)G_{inv}(z)|$

$|C_{prc}(z)G_{inv}(z)|$ denotes the open loop gain of the plug-in repetitive control system. In particular, the magnitude of $|C_{prc}(z)G_{inv}(z)|$ at the frequencies of the fundamental as well as high order harmonics determines the steady state tracking error. $|C_{prc}(z)G_{inv}(z)|$ is plotted in Fig. 7. It can be observed that the open loop gain peaks are higher than 40 dB and 20 dB at the harmonic frequencies up to the 9th order and 13th order respectively, which yields an excellent harmonic rejection capability.

V. BOOST-HALF-BRIDGE CONVERTER CONTROL

TABLE II summarizes the key parameters of the boost-half-bridge DC-DC converter. As aforementioned, the PV voltage is regulated instantaneously to the command generated by the MPPT function block. The PV voltage regulator is designed based on L_{in} and C_{in}. The continuous-time control block diagram is included in Fig. 3. High bandwidth PI control is adopted to track the voltage reference v_{pv}^* and minimize the double-line-frequency disturbance from the LVS DC link. The capacitor voltage differential feedback is introduced for active damping of the input LC resonance [39].

TABLE II
BOOST-HALF-BRIDGE CONVERTER PARAMETERS

Input PV voltage	$30V \sim 50V$
Nominal PV power	$210W$
Switching frequency	$21.6kHz$
LVS DC link voltage	$63V$
Transformer turns ratio	$1:6$
Transformer magnetizing inductors	$0.7mH : 25.2mH$
Input inductor (L_{in})	$200\mu H$

Typically, the MPPT function block in a photovoltaic converter/inverter system periodically modifies the tracking reference of the PV voltage, or the modulation index, or the converter duty cycles. In most cases, these periodic perturbations yield step change dynamic responses in power converters such that LC oscillation, inrush current and magnetic saturation may take place. Consequently, the conversion efficiency can be deteriorated or even malfunction of the converter may occur.

Eq. (1) and (2) indicate that $v_{c1} \sim v_{c4}$ are changing dynamically in accordance with d_1. It is worth noting that the charge and discharge of $C_1 \sim C_4$ caused by the uneven voltage distribution on the upper capacitors (C_1 and C_3) and the lower capacitors (C_2 and C_4) can only be conducted through the transformer magnetizing inductor. As a result, at any time, the charge and discharge rate of $C_1 \sim C_4$ must be limited such that the transformer flux is not saturated. Intuitively, this can be done by either introducing the transformer flux as a state variable into the inner PV voltage regulator or designing the outer MPPT block adaptively. For the sake of control simplicity and low cost, an MPPT method that generates a ramp-changed voltage reference is incorporated in practice in order to eliminate undesired dynamic responses associated with the MPPT operation.

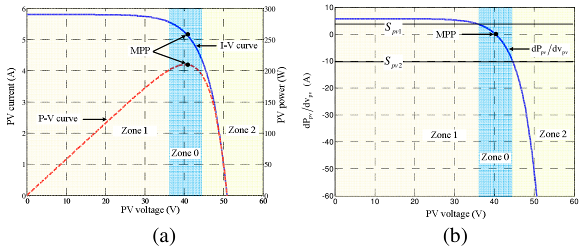

Fig. 8. (a) I-V, P-V curves. (b) PV operation zone division based on dP_{pv}/dv_{pv} .

For simplicity, it is assumed that the PV module is working under the standard irradiance ($1000\ \text{W/m}^2$) and the room temperature (25°C). Fig. 8(a) sketches the operation curves of Sanyo HIT-210N, which best fits the proposed micro inverter. In Fig. 8(b), dP_{pv}/dv_{pv} is illustrated. It is worth mentioning that some MPPT techniques calculate the step size online relying on the instantaneous values of ΔP_{pv} and Δv_{pv} in order to make the MPPT more adaptive [3], [27]. However, the sensed ΔP_{pv} and Δv_{pv} are vulnerable to noises, particularly when they are small. Therefore, an alternative method is adopted for robustness. Two points S_{pv1} and S_{pv2} on the dP_{pv}/dv_{pv} curve are selected to divide the PV operating points into three different zones, as Fig. 8(b) shows. In Zone 0, PV output power is close to the MPP, where a fine tracking step size is used to approach the exact MPP. In Zone 1 and Zone 2, a larger tracking step size is applied to boost up the tracking speed.

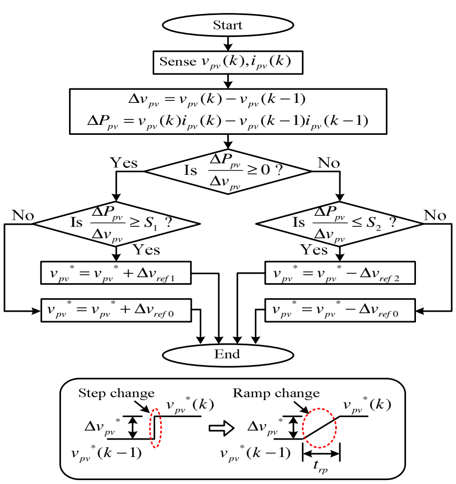

Fig. 9. Flow chart of the variable step size MPPT.

Fig.9 shows the proposed MPPT algorithm. $\Delta v_{ref0}, \Delta v_{ref1}$ and Δv_{ref2} represent the tracking step sizes in Zone 0, Zone 1 and Zone 2 respectively. k denotes the iteration number. In practice, Δv_{ref0}, Δv_{ref1} and Δv_{ref2} are selected as 0.1 V, 0.3 V and 0.3 V, respectively. The PV voltage reference v_{pv}^* is updated every 150 ms.

VI. Experimental Results

A 210 W boost-half-bridge PV micro inverter has been built and experimentally tested in the laboratory. The micro inverter is controlled by the 32-bit digital signal processor (TI TMS320F28035). One Sanyo PV module (HIT-210N) is selected as the low voltage power source. The validity of the boost-half-bridge DC-DC converter, the plug-in repetitive current controller, and the variable step size MPPT method are verified by the following experimental results.

A. Verification of the Boost-Half-Bridge DC-DC Converter

The experimental waveforms of the boost-half-bridge DC-DC converter are obtained in Fig. 10. In Fig. 10(a), the PV voltage is regulated to 36.8 V and the PV power is 190 W. In Fig. 10(b), the PV voltage and power are 44.5 V and 84 W, respectively.

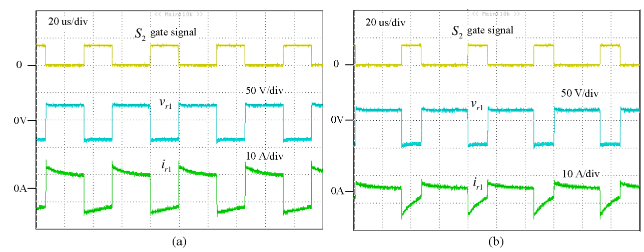

Fig. 10. Transformer voltage and current responses of the boost-half-bridge converter. (a) $P_{pv} = 190$ W , $v_{pv} = 36.8$ V . (b) $P_{pv} = 74$ W , $v_{pv} = 44.5$ V .

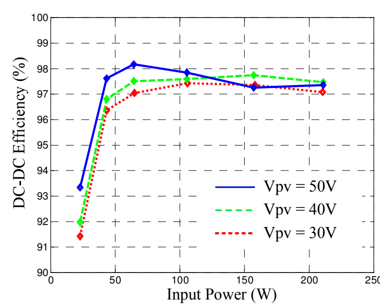

Fig. 11. Efficiency chart of the boost-half-bridge DC-DC converter.

The conversion efficiency of the boost-half-bridge main circuit is summarized in Fig. 11. It is measured based on the different input PV voltages and power levels. High efficiency (97.0%~98.2%) is achieved over the entire input voltage range (30 V~50 V) when the PV power is above 30% of the nominal value. The peak efficiency is measured as 95.6% at $P_{pv} = 160$ W and $v_{pv} = 40$ V when the full-bridge inverter is included.

B. Verification of the Plug-in Repetitive Current Regulator

The steady state grid voltage and current waveforms are depicted in Fig. 12. Both heavy load and light load conditions are tested to verify the current controller performance. As can be seen from Fig. 12(a), the proposed plug-in RC achieves a THD as low as 0.9% and a high power factor of 0.998 under heavy load. Low THD (2.87%) and high power factor (0.99) are still obtained even when the load is reduced by 2/3, as shown in Fig. 12(b).

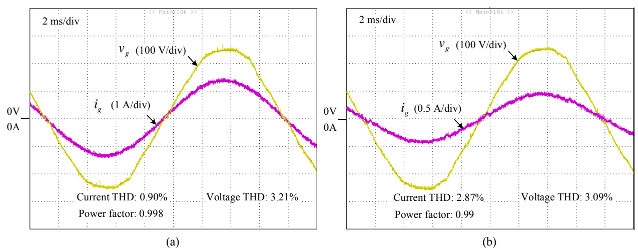

Fig. 12. Steady state grid voltage and current. (a) Heavy load. (b) Light load.

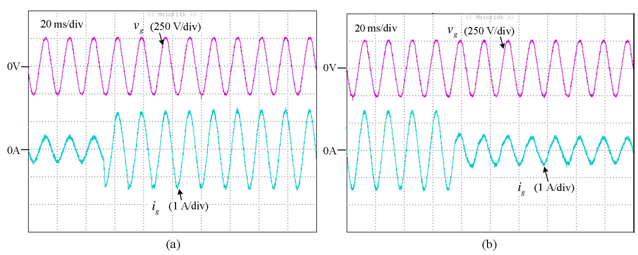

Fig. 13. Transient responses of the micro inverter system under load step change. (a) Grid current step change (0.33 A to 1 A). (b) Grid current step change (1 A to 0.33 A).

Dynamic responses of the plug-in RC are verified by the experimental results in Fig. 16. Fig. 16(a) and (b) show the results when the full-bridge inverter is tested independently. In Fig. 16(a) and (b), the grid current reference is step changed from 0.33 A to 1 A and 1 A to 0.33 A, respectively. The proportional part in the plug-in RC enables the controller to respond to the abrupt reference change promptly. Meanwhile, the RC part cancels the harmonic distortions in several fundamental cycles following the step change.

C. Verification of the Variable Step Size MPPT

As discussed in Chapter V, the variable step size MPPT with ramp-changed PV voltage reference is implemented experimentally. The MPPT response under solar irradiance change (partial shading to $880\ \mathrm{W/m^2}$) is presented in Fig. 14. It can be seen that the MPPT employs a larger step size 0.3 V right after the solar irradiance change to achieve fast tracking speed, and then shifts to a smaller step size 0.1 V for fine tracking. The steady state performance of the MPPT is verified by Fig. 15. The PV voltage oscillates around the MPP within a very small range (0.5 V) at the steady state, providing an MPPT efficiency higher than 99.7%.

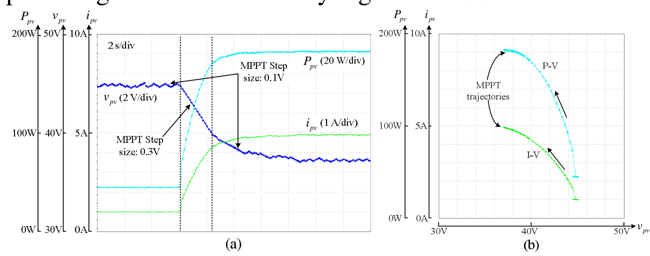

Fig. 14. MPPT of the PV micro inverter system under solar irradiance change. (a) PV voltage, PV current and PV power under solar irradiance change (partial shading to $880\ \mathrm{W/m^2}$ @ $50^{\circ}\mathrm{C}$). (b) MPPT trajectories (P-V and I-V curves).

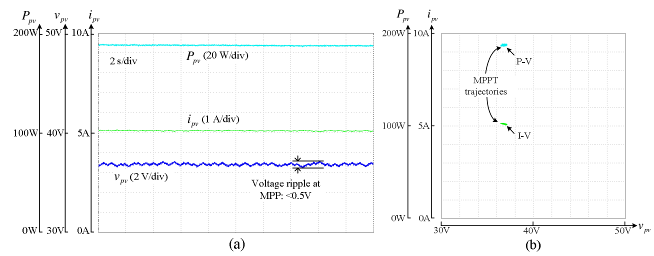

Fig. 15. MPPT of the PV micro inverter system at the steady state. (a) PV voltage, PV current and PV power (solar irradiance: $900\ \mathrm{W/m^2}$ @ $50^{\circ}\mathrm{C}$) (b) MPPT trajectories (P-V and I-V curves).

VII. Conclusion

A novel boost-half-bridge micro inverter for grid-connected photovoltaic systems has been presented in this paper. A plug-in repetitive current controller was proposed and illustrated. A variable step size MPPT control method was developed. Simulation and experimental results of the 210 W prototype were shown to verify the circuit operation principles, current control and MPPT method.

Thanks to the minimal use of semiconductor devices, circuit simplicity and easy control, the boost-half-bridge PV micro inverter possesses promising features of low cost and high reliability. According to the experimental results, high efficiency (97.0%~98.2%) is obtained with the boost-half-bridge DC-DC converter over a wide operation range. Moreover, the current injected to the grid is regulated precisely and stiffly. High power factor (> 0.99) and low THD (0.9%~2.87%) are obtained under both heavy load and light load conditions. Finally, the variable step size MPPT method provides a fast tracking speed and a high MPPT efficiency (> 99.7%). As a result, the proposed boost-half-bridge PV micro inverter system with its advanced control implementations will be a competitive candidate for grid-connected photovoltaic applications.

References

[1] S. B. Kjaer, J. K. Pedersen and F. Blaabjerg "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1292-1306, Sep/Oct. 2005.

[2] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1320-1333, May. 2008.

[3] R. Wai and W. Wang, "Grid-connected photovoltaic generation system," *IEEE Transactions on Circuits and Systems-I*, vol. 55, no. 3, pp. 953-963, Apr. 2008.

[4] M. Andersen and B. Alvsten, "200 W low cost module integrated utility interface for modular photovoltaic energy systems," in *Proc. IEEE IECON*, 1995, pp. 572–577.

[5] A. Lohner, T.Meyer, and A. Nagel, "A new panel-integratable inverter concept for grid-connected photovoltaic systems," in *Proc. IEEE ISIE*, 1996, pp. 827–831.

[6] D. C. Martins and R. Demonti, "Grid connected PV system using two energy processing stages," in *Proc. IEEE Photovoltaic Specialists Conf.*, 2002, pp. 1649-1652.

[7] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the dc input for an ac photovoltaic module system," *IEEE Trans. Power Electron.,* vol. 21, no. 5, pp. 1264–1272, Sep. 2006.

[8] N. Kasa, T. Iida, and L. Chen, "Flyback inverter controlled by sensorless current MPPT for photovoltaic power system," *IEEE Trans. Ind. Electron*., vol. 52, no. 4, pp. 1145–1152, Aug. 2005.

[9] Q. Li and P.Wolfs, "A current fed two-inductor boost converter with an integrated magnetic structure and passive lossless snubbers for photovoltaic module integrated converter applications," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 309–321, Jan. 2007.

[10] S. B. Kjaer and F. Blaabjerg, "Design optimization of a single phase inverter for photovoltaic applications," in *Proc. IEEE PESC, 2003*, pp. 1183–1190.

[11] H. Li, F. Z. Peng and J. S. Lawler, "Modeling, simulation, and experimental verification of soft-switched bi-directional dc-dc converters," in *Proc. IEEE APEC, 2001*, pp. 736–742.

[12] F. Z. Peng, H. Li, G. Su and J. S. Lawler, "A new ZVS bidirectional DC–DC converter for fuel cell and battery application," *IEEE Trans. Power Electron.,* vol. 19, no. 1, pp. 54–65, Jan. 2004.

[13] H. Li and F. Z. Peng, "Modeling of a new ZVS bi-directional dc-dc converter," *IEEE Transactions on Aerospace and Electronic Systems,* vol. 40, no. 1, pp. 272–283, Jan. 2004.

[14] D. Liu and H. Li, "A ZVS bi-directional DC–DC converter for multiple energy storage elements," *IEEE Trans. Power Electron.,* vol. 21, no. 5, pp. 1513–1517, Sep. 2006.

[15] C. Yoon, J. Kim and S. Choi, "Multiphase DC–DC converters using a boost-half-bridge cell for high-voltage and high-power applications," *IEEE Trans. Power Electron.,* vol. 26, no. 2, pp. 381–388, Feb. 2011.

[16] K. Zhang, Y. Kang, J. Xiong and J. Chen, "Direct repetitive control of SPWM inverters for UPS purpose" *IEEE Trans. Power Electron.,* vol. 18, no. 3, pp. 784–792, May. 2003.

[17] Y.-Y. Tzou, R.-S. Ou, S.-L. Jung, and M.-Y. Chang, "High-performance programmable AC power source with low harmonic distortion using DSP-based repetitive control technique," *IEEE Trans. Power Electron*., vol. 12, no. 4, pp. 715–725, Jul. 1997.

[18] K. Zhou and D. Wang, "Digital repetitive learning controller for three-phase CVCF PWM inverter," *IEEE Trans. Ind. Electron*., vol. 48, no. 4, pp. 820–830, Aug. 2001.

[19] G. Escobar, A. A. Valdez, J. Leyva-Ramos, and P. Mattavelli, "Repetitive-based controller for a UPS inverter to compensate unbalance and harmonic distortion," *IEEE Trans. Ind. Electron*., vol. 54, no. 1, pp. 504–510, Feb. 2007.

[20] S. Jiang, D. Cao, Y. Li, J. Liu and F. Z. Peng, "Low THD, fast transient, and cost-effective synchronous-frame repetitive controller for three-phase UPS inverters," in *Proc. IEEE ECCE,* 2011, pp. 2819-2826.

[21] P. Mattavelli and F. P. Marafao, "Repetitive-based control for selective harmonic compensation in active power filters," *IEEE Trans. Ind. Electron*., vol. 51, no. 5, pp. 1018–1024, Oct. 2004.

[22] R. Griñó, R. Cardoner, R. Costa-Castelló, and E. Fossas, "Digital repetitive control of a three-phase four-wire shunt active filter," *IEEE Trans. Ind. Electron*., vol. 54, no. 3, pp. 1495–1503, Jun. 2007.

[23] X. H. Wu, S. K. Panda, and J. X. Xu, "Design of a plug-in repetitive control scheme for eliminating supply-side current harmonics of three-phase PWM boost rectifier under generalized supply voltage conditions," *IEEE Trans. Power Electron*., vol. 25, no. 7, pp. 1800–1810, Jul. 2010.

[24] B. A. Francis and W. M. Wonham, "The internal model principle for linear multivariable regulators," *Appl. Math. Opt.,*, vol. 2, pp. 170-194, 1975.

[25] L. Li, L. Xie, W. Yan and Y. C. Soh, "Design of low-order linear-phase IIR filters via orthogonal projection" *IEEE Trans. Signal Processing*, vol. 47, no. 2, pp. 448–457, Feb 1999.

[26] E. Koutroulis, K. Kalaitzakis, and N. C. Voulgaris, "Development of a microcontroller-based, photovoltaic maximum power point tracking control system," *IEEE Trans. Power Electron.,* vol. 16, no. 21, pp. 46–54, Jan. 2001.

[27] A. K. Abdelsalam, A. M. Massoud, S. Ahmed and P. Enjeti, "High-performance adaptive perturb and observe MPPT technique for photovoltaic-based microgrids," *IEEE Trans. Power. Electron*., vol. 26, no. 4, pp. 1010–1021, Apr. 2011.

[28] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," *IEEE Trans. Power Electron*., vol. 20, no. 4, pp. 963–973, Jul. 2005.

[29] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "A technique for improving P&O MPPT performances of double-stage grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.,* vol. 56, no. 11, pp. 4473–4482, Nov. 2009.

[30] Y.-C. Kuo, T.-J. Liang, and J.-F. Chen, "Novel maximum-power-pointtracking controller for photovoltaic energy conversion system," *IEEE Trans. Ind. Electron*., vol. 48, no. 3, pp. 594–601, Jun. 2001.

[31] Y. H. Lim and D. C. Hamill, "Simple maximum power point tracker for photovoltaic arrays," *Electron. Lett.,* vol. 36, pp. 997–999, May 2000.

[32] H. Patel and V. Agarwal, "MPPT scheme for a PV-fed single-phase single-stage grid-connected inverter operating in CCM with only one current sensor," *IEEE Trans. Energy Conv*., vol. 24, no. 1, pp. 256–263, Mar. 2009.

[33] S. Jain and V. Agarwal, "Comparison of the performance of maximum power point tracking schemes applied to single-stage grid-connected photovoltaic systems," *IET Electr. Power Appl.,* vol. 1, no. 5, pp. 753–762, Sep. 2007.

[34] T. Esram and P. L.Chapman, "Comparison of photovoltaic arraymaximum power point tracking techniques," *IEEE Trans. Energy Conv*., vol. 22, no. 2, pp. 439–449, Jun. 2007.

[35] E. Twining and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. Power. Electron*., vol. 18, no. 3, pp. 888–895, May. 2003.

[36] G. Shen, D. Xu, L, Cao and X. Zhu, "An improved control strategy for grid-connected voltage source inverters with an LCL filter," *IEEE Trans. Power Electron.,* vol. 23, no. 4, pp. 1899–1906, Jul. 2008.

[37] M. Liserre, F. Blaabjerg and S. Hansen, "Design and control of an LCL-filter-based three-phase cctive rectifier," *IEEE Transactions on Industry Applications,* vol. 41, no. 5, pp. 1281-1291, Sep/Oct. 2005.

[38] J. Dannehl, M. Liserre and F. W. Fuchs, "Filter-based active damping of voltage source converters with LCL filter," *IEEE Trans. Ind. Electron*., vol. 58, no. 8, pp. 3623–3633, Aug. 2011.

[39] S. Yang, X. Ding, J. Liu and Z. Qian, "Analysis and design of a cost-effective voltage feedback control strategy for EPS inverters," in *Proc. IEEE PESC, 2007*, pp. 477–482.