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Three-level NPC inverter based new DSTATCOM topologies and their performance evaluation for load compensation

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ABSTRACT

Now-a-days for effective load compensation, a conventional three-level neutral point clamped (CNPC) inverter topology is more preferably used. This compensator, however, faces the problems of additional clamping diodes, which reduces the redundant switching states and improves the problem of capacitor voltage imbalance; further increasing the inverter cost. In this paper, a detailed analysis of conventional NPC voltage source inverter (VSI) based Distribution Static Compensator (DSTATCOM) is given for shunt applications and to overcome its limitations, Conergy NPC and Active NPC VSI based new DSTATCOM topologies are proposed, exclusively for the load compensation. To demonstrate the effectiveness of the aforementioned topologies for shunt compensation, a three phase four wire system has been taken into consideration. Instantaneous symmetrical component theory (ISCT) is used for reference current generation, while, the hysteresis current control pulse width modulation (PWM) is used to generate the switching sequence for all the NPC configurations. A detailed simulation study has been carried out in MATLAB environment and the comparative evaluation of all the above DSTATCOM topologies is being provided.

Introduction

DSTATCOM is a VSI based shunt connected popular custom power device, used to achieve load compensation [1]. The various DSTATCOM configurations using conventional and multilevel inverters with its detailed control, working and analysis are discussed in literature [2–5]. In VSI applications, two-level split capacitor configuration can compensate unbalance loads containing zero sequence components [6]; but imbalances the capacitor voltages. Further, this imbalance becomes more rapid if the load current contains dc component. Hence, chopper circuit needs to be used for capacitor voltage balancing. However, in the two level VSI, determination of chopper inductor rating becomes more complex. To alleviate such problem in shunt applications, it is suggested to use a three-level conventional NPC inverter [7], in which, there is no voltage drift during zero voltage state; thus, bypassing the capacitors. The investigations showed that NPC inverter is a promising alternative for high, medium and low voltage applications [8] with superior output voltage quality. Though popular and most advantageous topology, conventional NPC inverter also has certain drawbacks [9] such as: neutral point potential divergence, unequal distribution of semiconductor losses among the devices, indirect clamping of inner devices, blocking voltages of clamping diodes and impractical use of large clamping diodes due to diode reverse recovery. To overcome above limitations to some extent, alternate NPC topologies are suggested [10]; which can replace the conventional 3-level NPC configuration for shunt compensation.

In this paper, Conergy NPC inverter [11] (which is a typical grid connected PV based transformerless VSI topology) based new DSTATCOM topology is proposed, exclusively for load compensation. It is a variant of CNPC, patented by conergy in 2007, but emerged as a different VSI topology. This topology overcomes the limitation of clamping diode as needed in CNPC. Also, the major drawback of CNPC is the unequal load distribution among the semiconductors. Due to which, the losses in the most stressed devices limit the switching frequency and the output power of the converter. Thus, to achieve, an appropriate loss distribution and better semiconductor utilization, Active NPC (ANPC) inverter (claimed as new topology) [12] based new DSTATCOM topology, which combines the flexibility of FC with robustness of 3-level conventional NPC, is also proposed. This topology allows the new switching states without clamping diodes with consequently proper semiconductor loss balancing [13,14].

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For all the above three NPC configurations i.e. conventional, Conergy, and active NPC based DSTATCOM, the switching sequence is developed using hysteresis current control PWM due to its multiple advantages [15–17]. The various control algorithms are already proposed [18–21] for generation of DSTATCOM reference currents. Here, the DSTATCOM reference currents are extracted using instantaneous symmetrical component theory [22]. An extensive digital simulation has been carried out for the comparative evaluation of all the three configurations using DSTATCOM applications for load compensation. Among various schemes [23,24], an open loop duty cycle control is found easy for implementation. As well as, simulation study shows that, in terms of settling time, THD in source currents and capacitor voltage ripples; it performs better as compared to closed loop control. Hence, the open loop duty cycle control [24] is realized for external chopper circuit to overcome the effect of capacitor voltage imbalance, for all the topologies. However, the conventional NPC inverter based DSTATCOM, under balanced as well as unbalanced capacitor voltages is discussed in Section 4 and other two proposed topologies are discussed under balanced capacitor voltages. The simulation results show that the control algorithm works satisfactorily for all the topologies and effectively compensate the source currents with unity power factor (UPF). Amongst all, the Active NPC seems to be most suitable DSTATCOM topology for shunt applications.

DSTATCOM Topologies

This section describes the various NPC inverter based DSTATCOM topologies. The VSI can be realized using any switching device having reverse conducting capability. In simulation study, IGBT with anti-parallel diode is used as a switch. When the switches are blocked, the dc capacitor charges to peak value of ac voltage through anti-parallel diodes. All the NPC VSI topologies discussed are used for low voltage 3-phase 4-wire (3p4w) distribution system without the isolation transformer. A basic block diagram of DSTATCOM structure is shown in Fig. 1.

Conventional NPC VSI based DSTATCOM

Fig. 2 shows a 3p4w DSTATCOM structure for load compensation. The DSTATCOM is realized using 3-leg, 3-level conventional NPC (CNPC) VSI (also known as classical NPC). Each leg has four switches (S_{1a}, S_{2a}, S_{3a}, S_{4a}), two clamping diodes (D_{a+}, D_{a-}) and two dc capacitors (C_{dc1}, C_{dc2}). The neutral of two capacitors (n'), the neutral of source (N) and the neutral of the load (n) are connected together. The zero voltage level can be achieved by 'clamping' the output to the grounded 'middle point' of the dc link

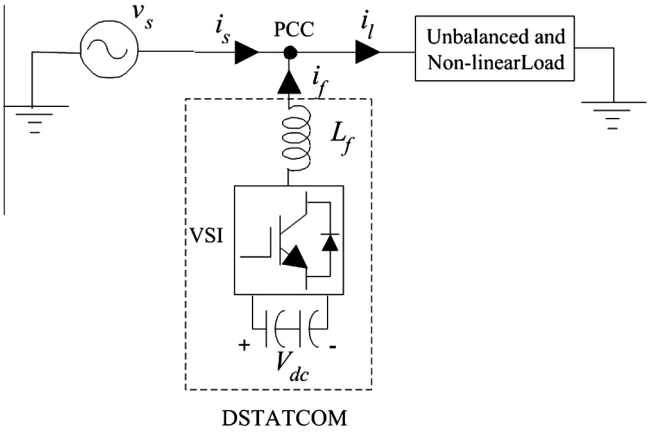

Fig. 1. Basic DSTATCOM structure.

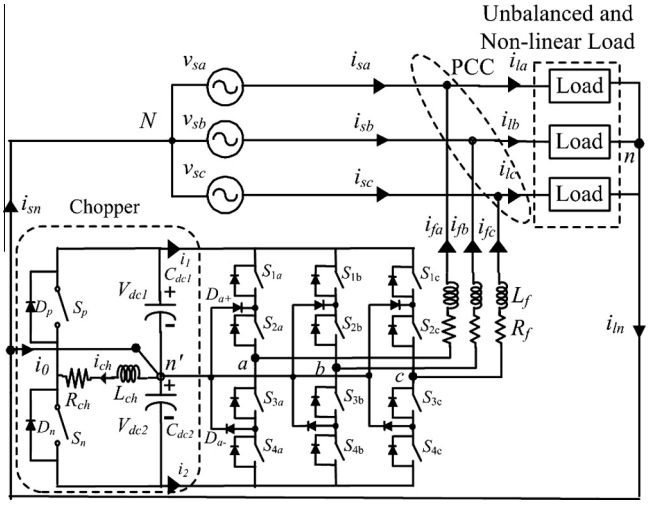

Fig. 2. DSTATCOM using CNPC inverter.

capacitors using clamping diodes, depending on the direction of the current. The main feature of this converter is that the outer switches (S_{1a}, S_{4a}) are switched at the higher switching frequency while, the inner switches (S_{2a}, S_{3a}) switched at the system frequency. This topology usually provides the higher efficiency, reduced switching losses and very low leakage current and electromagnetic interference (EMI) compared to conventional two level inverter [11]. The switching sequence to achieve three levels (V_{dc1}, 0, V_{dc2}) is given in Table 1.

Conergy NPC VSI based DSTATCOM

Conergy NPC is also known as multi neutral point clamped (MNPC) VSI. It is a variant of three-level classical NPC, with output clamped to the neutral, using bidirectional switch, realized using two series back-to-back IGBTs. The bidirectional switch can also be realized with the several combinations of switch technology. Since it has to block only half of the dc-link voltage, it is possible to use switches with half of the blocking voltage rating. The main features of this converter are: It eliminates the need of the additional clamping diodes (reducing the cost and complexity of the topology), S_{1a} (S_{2a}) and S_{a+} (S_{a-}) are switched at higher frequencies and two zero voltage states are obtained, provides balanced switching losses as compared to conventional NPC and produces very low leakage current and EMI. No reactive power exchange between L_f and C_{dc1}, C_{dc2} during zero voltage state and reduced voltage drop, as only one switch is conducting during active state; results in the higher efficiency.

A 3p4w compensator structure considered for shunt applications is realized using 3-level 3-leg Conergy NPC VSI as shown in Fig. 3. Each leg consists of four switches with anti-parallel diodes connected across it. The mid-point (n') of the two split capacitors are connected to neutral wire N–n of the system. The three switching states ($+V_{dc1}$, 0, $-V_{dc2}$) are shown in Table 2.

Table 1
Switching scheme for conventional NPC VSI.

S_{1a}	S_{2a}	S_{3a}	S_{4a}	D_{a+}	D_{a-}	V'_{an}
ON	ON	OFF	OFF	OFF	OFF	$+V_{dc1}$
OFF	ON	OFF	OFF	ON	OFF	0 }
OFF	OFF	ON	OFF	OFF	ON	0 }
OFF	OFF	ON	ON	OFF	OFF	$-V_{dc2}$

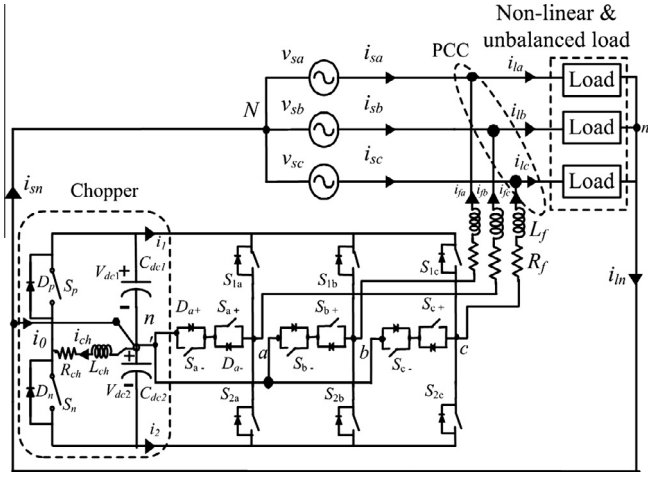

Fig. 3. DSTATCOM using MNPC inverter.

Table 2
Switching scheme for MNPC VSI.

S_{1a}	S_{2a}	S_{a-}	S_{a+}	D_{a+}	D_{a-}	V'_{an}
ON	OFF	OFF	OFF	OFF	OFF	$+V_{dc1}$
OFF	OFF	OFF	ON	ON	OFF	0
OFF	OFF	ON	OFF	OFF	ON	0
OFF	ON	OFF	OFF	OFF	OFF	$-V_{dc2}$

Active NPC VSI based DSTATCOM

Active NPC (ANPC) three-level VSI is a hybrid asymmetrical inverter structure which combines the flexibility of floating-capacitor with robust conventional neutral point clamped converter. In this topology, for the higher levels (more than three-levels), it is only required to balance the voltages across the dc link capacitors, where as the voltage across the floating capacitor is controlled based on the redundant switching states, reducing the balancing complexity as compared to the flying capacitor topology. As the number of achieved voltage level decreases the number of available per phase redundant states increases. Therefore, three level ANPC is generally used to achieve maximum redundant sates. Further, due to redundancy in switching states, ANPC has more degree

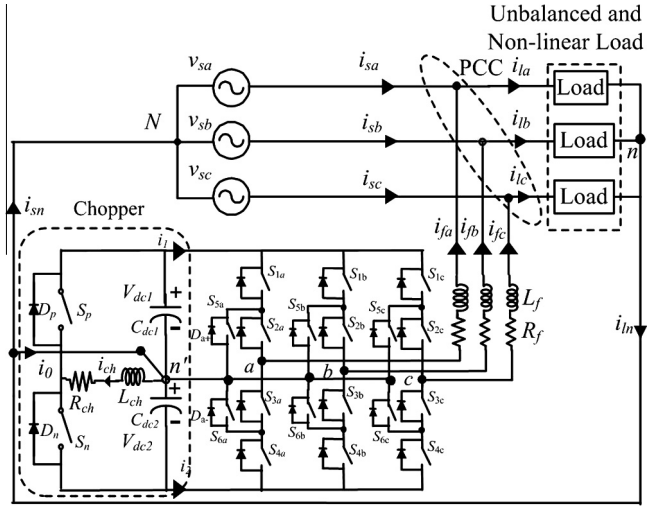

Fig. 4. DSTATCOM using ANPC inverter.

Table 3
Switching scheme for ANPC VSI.

S_{1a}	S_{2a}	S_{3a}	S_{4a}	S_{5a}	S_{6a}	D_{a+}	D_{a-}	V'_{an}
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	$+V_{dc1}$
OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	0
OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	0
OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	0
OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	0
OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	$-V_{dc2}$

of freedom and can be controlled using different PWM strategies [14].

Fig. 4 shows a circuit for 3-level active NPC based DSTATCOM. The neutral of source, load and compensator are connected together to form 3p4w DSTATCOM structure. It consists of six switches (per phase) provided with the anti-parallel diodes and the two split capacitors. Elimination of clamping diode in ANPC provides important advantage like flexible switching strategies and also has the zero voltage state used to reduce the conduction losses which further improve the converter efficiency. The three voltage states that can be obtained through redundant switching are given in Table 3. Here, Table 4 shows the comparison of component count requirement for all the three topologies.

In this paper, all the NPC topologies are realized with conventional dc-dc two quadrant chopper circuit, for capacitor voltage balancing as shown in Figs. 2–4. However, an open loop duty cycle control strategy is implemented for chopper control, for all the topologies. The chopper consists of inductor L_{ch} used to exchange the energy between C_{dc1} and C_{dc2} using two switches S_p, S_n and diodes D_p, D_n. In order to evaluate the exchange of energy between the capacitors, chopper will have to restore the capacitor voltages to their respective reference values (V_{dcref1}, V_{dcref2}). For the faster rate of transfer of energy, the L_{ch} must be selected to a very low value.

It is to be noted that along with nullifying the effect of clamping diodes, the major benefits of 3-level conventional NPC is retained in both MNPC and ANPC topologies by maintaining the voltage rating of each of the switch in the main leg same as CNPC. Only for the sake of verification of the switching losses and efficiency of the VSI schemes, comparison in the terms of number of switching per cycle are given in Table 6 however, loss calculations are beyond the scope of this paper.

Switching dynamics of VSI

Design of VSI and chopper parameters

The most crucial aspect for realization of DSTATCOM is the design of VSI parameters. The various vital parameters that needs to taken into consideration are dc-link voltage V_{dcref}, dc storage capacitors C_{dc1}, C_{dc2}, interfacing inductor L_f, switching frequency f_{sw}, hysteresis band h, dead band δ. A detailed design procedure of VSI parameters is given in [25]; based on the following equations, the parameters are chosen. The dc-link capacitor is given by (1)

$$C_{dc1} = C_{dc2} = \frac{(2X - X/2)nT}{(1.8V_m)^2 - (1.4V_m)^2} \tag{1}$$

where X is the kVA rating of the system, n is the number of cycles, T is the period of each cycle, and V_m is the peak value of the source voltage.

The interfacing inductor is given by (2)

$$L_f = \frac{mV_m}{4hf_{sw\max}} \tag{2}$$

Table 4
Comparison of multilevel NPC topologies in terms of component counts (per phase).

NPC topology	Voltage levels (m)	Main switches	Main diodes	Clamping diodes	Floating capacitors	DC link capacitors	Isolated DC sources
Conventional NPC (CNPC)	m	2(m – 1)	2(m – 1)	(m – 1)(m – 2)	0	(m – 1)	1
Conergy NPC (MNPC)	m	2(m – 1)	2(m – 1)	0	0	(m – 1)	1
Active NPC (ANPC)	m	2(m – 1)	2(m – l)	0	(m – 3)/2	2	1

where h is the hysteresis band given as

$$h = \frac{K_1(2m^2-1)}{K_2(4m^2)} f_{sw\max} \tag{3}$$

where K_1, K_2 are proportionality constants, $f_{sw\max}$ and $f_{sw\min}$ are the maximum and minimum switching frequencies of the switch. m is given by (4)

$$m = \frac{1}{\sqrt{1 - f_{sw\min}/f_{sw\max}}} \tag{4}$$

Accordingly the dc-link voltage for each capacitor is taken as

$$V_{dcref} = mV_m$$

The dead band (δ) is generally selected much lower than hysteresis band, nearly 5–10% of 'h'.

While designing a chopper the dc–dc converter is assumed to restore the capacitor voltage to V_{dcref} at a sufficiently fast rate. For this chopper inductor L_{ch} should be sufficiently small such that the transfer of energy from L_{ch} to C_{dc1}, C_{dc2} or vice versa occurs rapidly. During unbalance the extra energy stored in the dc-link capacitor is calculated as

$$E = \frac{1}{2}C_{dc}\left(V_{dcref} + \frac{\nabla}{2}\right)^2 - \frac{1}{2}C_{dc}V_{dcref}^2 \tag{5}$$

In this case, the maximum chopper current $i_{ch\max}$ can then be expressed as (6)

$$i_{ch\max} = \frac{V_{dcref}}{L_{ch}} T_{on} \tag{6}$$

where

$$T_{on} = \sqrt{\left\{\left(\frac{V_{dcref} + \nabla/2}{V_{dcref}}\right)^2 - 1\right\}} (L_{ch}C_{dc})^{1/2}$$

From (6), by selecting the maximum chopper current equal to the average neutral current, proper value of L_{ch} can be calculated.

Whereas, R_{ch} is considered to be very small, assuming that it is too small to make any significant impact.

Modulation control and compensation algorithm

Being popular, hysteresis modulation technique, with slight modification in switching pattern, is implemented for all the topologies.

To avoid the switching towards two level scheme, a dead band (δ) is introduced in the hysteresis band (h); keeping δ always lower than h, for minimizing tracking error. If 'S' is the switching function, then the generalized gating pulse generation logic for 3-level inverter is given by (1).

$$\left.\begin{array}{l} \text{If} \quad (i_{i_{ref}} - i_i) > 0 \text{ then,} \\ \qquad \text{For} \quad (i_{i_{ref}} - i_i) \geqslant h, S = 1 \\ \qquad \text{For} \quad (i_{i_{ref}} - i_i) \leqslant \delta, S = 0 \\ \text{Else if} \quad (i_{iref} - i_i) < 0 \text{ then,} \\ \qquad \text{For} \quad (i_{i_{ref}} - i_i) \leqslant -h, S = -1 \\ \qquad \text{For} (i_{i_{ref}} - i_i) \geqslant \delta, S = 0 \end{array}\right\} \tag{7}$$

where $i_i = i_a$, i_b, i_c and $i_{iref} = i_{aref}$, i_{bref}, i_{cref} are the actual, reference compensator currents for $i = a$, b, c phases respectively and $(i_{iref} - i_i)$ is the error signal. The switching dynamics and the switching states obtained using (7) are shown in Fig. 5.

In conventional NPC, the transition from lower (upper) to upper (lower) band occurs automatically, through only zero state; when the rate of fall (rise) of the reference current waveform is higher than the actual current. The hysteresis band is chosen based on the current ripple that can be tolerated in the band. Aforementioned logic is digitally used to develop switching pattern also for MNPC and ANPC inverter with slight alteration. In case of Conergy NPC, out of two high and two low pulses, only single high pulse is applied to uppermost switch; while two low pulses and one inverted high pulse are applied to the remaining three switches, so that as per its switching sequence, only one switch should be conducting during active state and remaining three switches should remain 'OFF' in each leg of VSI. In case of ANPC, similar to CNPC, initially upper two main switches are kept 'ON' by applying high pulses, while lower two switches kept 'OFF' with the help of low pulses. Since in this topology, additional two clamping switches are used, during initial state to obtain V_{dc1}, the intermediate switches are kept 'OFF' by applying same low pulses. Table 3 indicates the maximum available redundancies in three-level ANPC, one can choose a preferential switching state for these output voltage that will help in maintaining capacitor voltage. Here, the switching states selected to achieve zero voltage level for all the three topologies are same, which can be obtained as per the switching sequence described above.

For all the above DSTATCOM topologies, ISCT is used to generate the reference compensator currents given by (8).

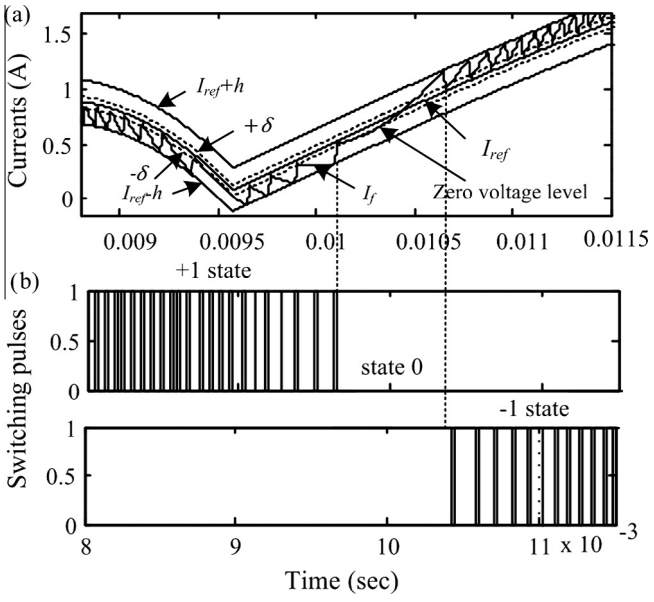

Fig. 5. Hysteresis PWM for 3-level NPC VSI (a) switching dynamics (b) switching pulses.

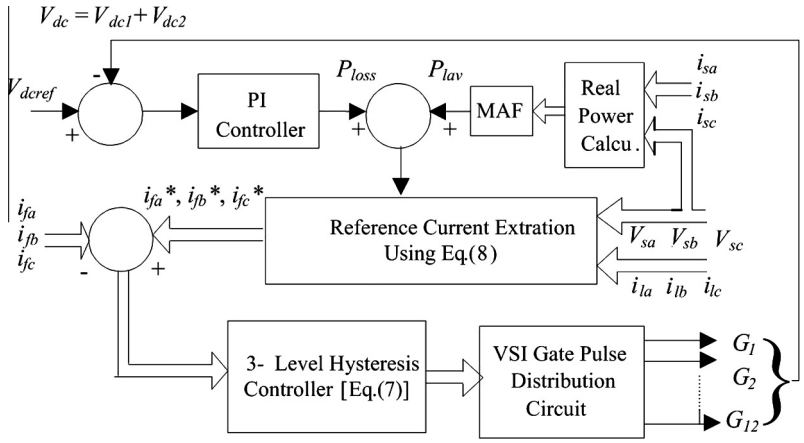

Fig. 6. DSTATCOM control scheme.

$$\left.\begin{aligned} i_{fa}^* &= i_{la} - i_{sa} = \frac{V_{sa}+\gamma(V_{sb}-V_{sc})}{\sum_{i=a,b,c} V_{si}^2}(p_{lavg} + p_{loss}) \\ i_{fb}^* &= i_{lb} - i_{sb} = \frac{V_{sb}+\gamma(V_{sc}-V_{sa})}{\sum_{i=a,b,c} V_{si}^2}(p_{lavg} + p_{loss}) \\ i_{fc}^* &= i_{lc} - i_{sc} = \frac{V_{sc}+\gamma(V_{sa}-V_{sb})}{\sum_{i=a,b,c} V_{si}^2}(p_{lavg} + p_{loss}) \end{aligned}\right\} \quad (8)$$

where γ is the required phase angle between source voltages (V_{sa}, V_{sb}, V_{sc}) and compensated source current (i_{sa}, i_{sb}, i_{sc}) respectively and given by $\gamma = \tan\phi/\sqrt{3}$. Hence γ is selected as zero for desired UPF operation. $P_{lavg} = V_{sa}i_{sa} + V_{sb}i_{sb} + V_{sc}i_{sc}$, represents average load power and is obtained by feeding the instantaneous load power to low pass filter. Inverter losses (P_{loss}) are generated using proportional-integral (PI) controller. In order that the capacitor must be capable to supply (absorb) power to (from) the ac system, even though, the capacitors have different voltages; the dc capacitor voltage error must be regulated through PI controller and the compensator performance remains unaffected to achieve desired load compensation. Let V_e be the voltage error between reference and actual dc capacitor voltage then,

$$V_e = V_{dcref} - V_{dc} \quad (9)$$

where $V_{dc} = V_{dc1} + V_{dc2}$

$$P_{loss} = K_p V_e + K_i \int V_e \cdot dt \quad (10)$$

Table 5
System parameters.

System parameters	Values (ratings)
Source voltages	Balanced sinusoidal V_{sa} = 230 V
Unbalanced load	$R_{la} + jX_{la}$ = l40 + j32.04 Ω $R_{lb} + jX_{lb}$ = 70 + j30.48 Ω $R_{lc} + jX_{lc}$ = 50 + j3.769 Ω
Non-linear load	(1) Three phase diode rectifier having a load of 298 + j31.41 Ω (2) Single phase diode rectifier having a load of 70 Ω connected between phase-a and load neutral
3-Level NPC (CNPC/ MNPC/ANPC) inverter	$C_{dc1} = C_{dc2}$ = 2200 μF $V_{dc\ ref}$ = 500 V
Interface inductor	R_f = 1 Ω, L_f = 30 mH
Hyst. band (h), dead band (δ)	h = ±0.21 A, δ = ±0.05 A
Chopper control	Switching frequency = 500 Hz, R_{ch} = 2 Ω, L_{ch} = 200 mH

where K_p and K_i are the proportional and integral gains of the PI controller.

A detailed control scheme based on Eqs. (7)–(10) for all the DSTATCOM topologies, is presented in Fig. 6.

Performance evaluation

Table 5 shows the system parameters used in simulation study and maintained same for all the topologies. The compensators performance evaluated through a digital simulation for shunt applications is summarized in the following subsections.

DSTATCOM performance using CNPC

A DSTATCOM with conventional NPC VSI shown in Fig. 2 is simulated for 3p4w system. The compensator is connected at the point of common coupling (PCC) through coupling inductor (L_f, R_f). It is always preferred to use the coupling transformer to isolate the VSI from load circuit. Since the paper incorporates transformerless topologies, isolation transformer is replaced by interface inductor L_f, which is equivalent to the leakage inductance of the transformer. The internal resistance of the inductor is represented by R_f, which is modeled as a summation of VSI switching losses and transformer copper loss (neglecting iron losses), which is further replenished by drawing extra real power from the source (P_{loss}). The system consists of unbalanced R–L load plus non-linear load realized using three-phase uncontrolled diode rectifier with R–L load drawing a current of 1.8 A. In order to introduce dc component, a single phase half-wave rectifier load of 70 Ω is added in phase-a.

When system contains unbalance load, the zero sequence current flows into the neutral point of the split dc capacitors, producing ripples in the capacitor voltages with the frequency of zero sequence components of the current. The dc component introduced by single phase half wave rectifier load will flow through path n–n', causing divergence and imbalance in the capacitor voltages. Further, the voltage of the discharge capacitor will fall to such a low value (below system peak), that the compensator becomes unable to achieve the satisfactory tracking performance.

Hence, when the source is balanced while, load is unbalanced and distorted, Fig. 7(a) shows the balanced and sinusoidal source voltages whereas, Fig. 7(b) represents unbalanced and distorted load/source currents (assuming source to be stiff) under uncompensated conditions with considerable neutral current. The dc component produces dc shift in the load current of phase-a. This

Table 6
Performance analysis of CNPC, MNPC and ANPC DSTATCOM topologies.

DSTATCOM topology	Source current (A)			Source current THD (%)			Power factor			Injected current (mean) (A)	Neutral current (A)	Switching frequency (kHz)		Average switching instants per cycle
	i_{sa}	i_{sb}	i_{sc}	a	b	c	a	b	c	i_f	i_{sn}	$f_{sw\ min}$	$f_{sw\ max}$	S_n
CNPC	3.485	3.483	3.502	1.915	2.586	3.778	1	1	1	1.671	0.2019	6.7	14.97	185
MNPC	3.402	3.461	3.487	2.427	2.216	2	0.99	0.99	1	1.652	0.2159	6.5	14.8	183
ANPC	3.484	3.485	3.483	1.975	1.943	1.887	1	1	1	1.62	0.1403	6.2	14.67	181

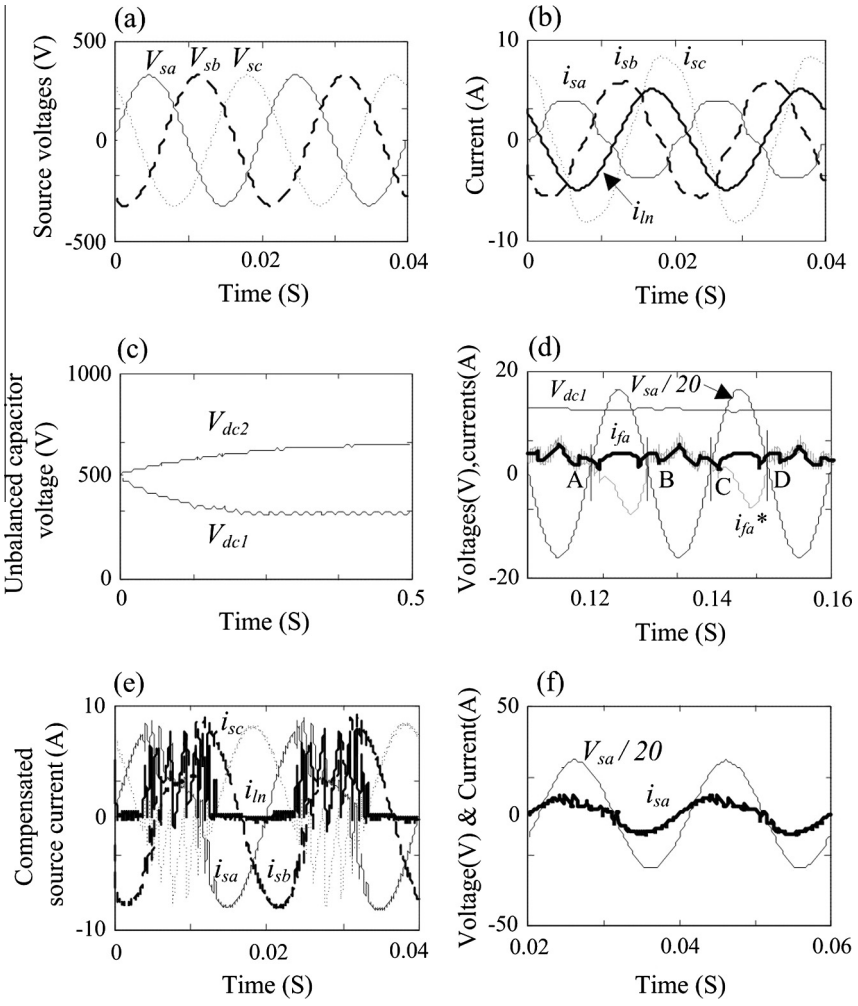

Fig. 7. Simulation results after compensation using CNPC without capacitor balancing (a) source voltages (b) source currents (c) capacitor voltages (d) loss of tracking (phase-a) (e) poor source current compensation (f) source voltage and source current.

dc component causes upper capacitor to undercharge while the lower to overcharge for positive dc component. Hence, the capacitor voltages continuously diverge as shown in Fig. 7(c) and there is loss of tracking performance observed between reference and actual compensator currents. The lower capacitor overcharged to 760 V, while the upper capacitor undercharged to 220 V. It is observed that when capacitor voltage falls below system peak between points A–B, C–D and so on, the compensator is unable to track the reference current as this depicts from Fig. 7(d). Therefore, it is evident from Fig. 7(e), (f) that the source currents get poorly compensated and also the source power factor (PF) is worsen during the poor tracking instants. It clearly shows that the source currents are distorted badly during the loss of tracking period with the partial neutral current compensation.

When the chopper circuit is activated, the capacitor voltages are regulated to their reference value 500 V as seen from Fig. 8(a). A negligible effect of ripples in the capacitor voltages is due to the presence of ac components in the neutral current. At this steady state stabilized dc capacitor voltages, the full compensation is provided by this topology. Hence, balanced and sinusoidal source currents with almost zero neutral current and UPF are obtained as shown in Fig. 8(b), (d). The source voltages are scaled down by the factor 20 in order to show the effective phase relationship between source current and voltage. From Fig. 8(c), it can also be depicted that, under the regulated capacitor voltages, the compensator currents exactly tracks the reference currents for all the three phases. Fig. 8(e) shows the peak chopper current of 6.5 A, which is averagely equal to neutral current, indicates that the compensator

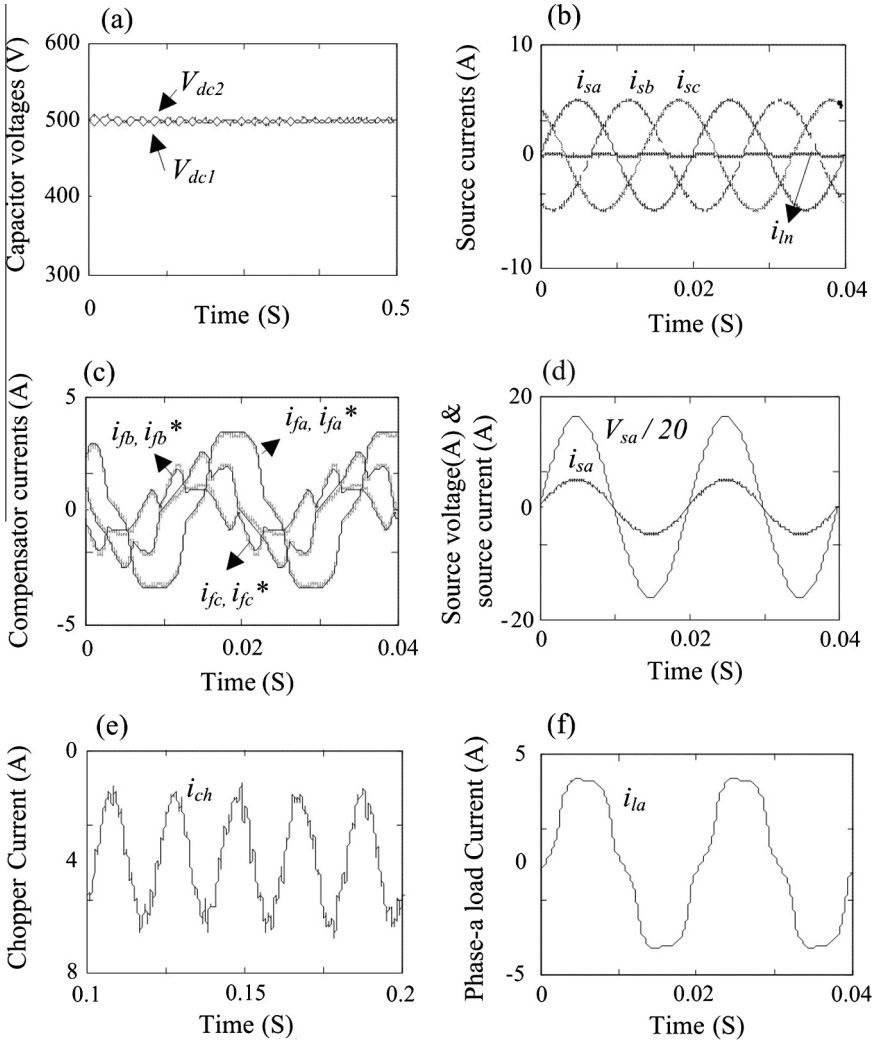

Fig. 8. Simulation results after compensation using CNPC DSTATCOM with capacitor balancing (a) capacitor voltages (b) source currents (c) compensator and reference injected currents (d) source voltage and source current (phase-a) (e) chopper current (f) phase-a load current.

is able to nullify the effect of dc component in the load current by maintaining proper value of duty cycle during steady state. The dc shift introduced in the phase-a load current due to a single phase half wave diode rectifier is also shown in Fig. 8(f). It is observed that the chopper control is able to remove this dc shift effectively, maintaining the capacitor voltages at their reference values and further improving the source current waveforms.

DSTATCOM performance using MNPC

Keeping the loading conditions same and replacing the compensator structure with Conergy NPC VSI with the same system parameters mentioned in Table 5, the system is again simulated and studied for 3p4w structure. It is seen that under unbalanced and balanced capacitor voltages, its behavioral trend is similar to conventional NPC VSI based DSTATCOM. With the chopper control circuit, once the capacitor voltages are equalized, it is evident from Fig. 9(a), (b) that source voltages and the source currents are found to be balanced and sinusoidal with completely eliminating the effect of zero sequence and dc component from neutral current. Fig. 9(c) shows the corresponding compensator currents which are found to be exactly tracking the reference currents. The injected currents are seen to be distorted in nature, since the loads are also distorted. It is depicted in Fig. 9(d) that this topology is also able to provide almost the UPF.

DSTATCOM performance using ANPC

When ANPC VSI based DSTATCOM topology is evaluated with the same system specifications, an improved system performance is observed and its corresponding results are shown in Fig. 10. Using the two quadrant chopper scheme, when the divergence in the capacitor voltage is avoided, better control over the source currents, neutral current and PF can be achieved. It is seen from Fig. 10(a) that the source currents become balanced and sinusoidal with almost zero neutral current. The corresponding injected currents by compensator are shown in Fig. 10(b). It is observed from Fig. 10(c) that the compensator currents are exactly tracking the reference currents (shown for phase-a). Here the results are shown on phase-a basis to show the effectiveness of the compensator even under large dc components which are added to phase-a load current. Since the hysteresis control has been used, it shows the variation in switching frequency (f_{sw}) between 6 and 15 kHz. It is observed that the minimum and maximum switching frequencies occur near the positive and the negative peaks of the system voltage respectively. Further, it is seen that ANPC VSI is able to change the switching frequency in order to track the sudden

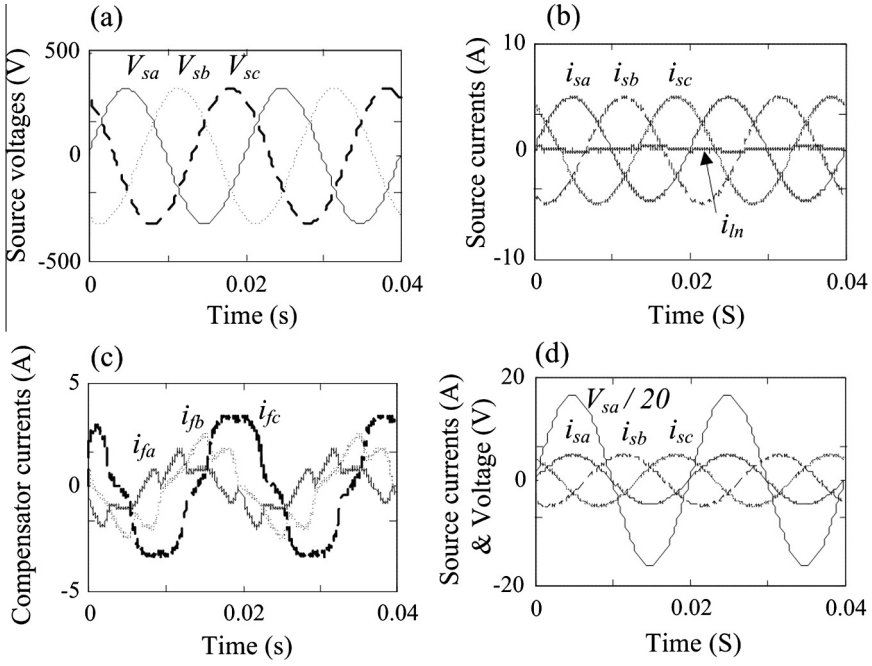

Fig. 9. Simulation results with Conergy NPC DSTATCOM (a) source voltages (b) source currents with neutral current (c) compensator injected currents (d) source voltage (phase-a) and source currents.

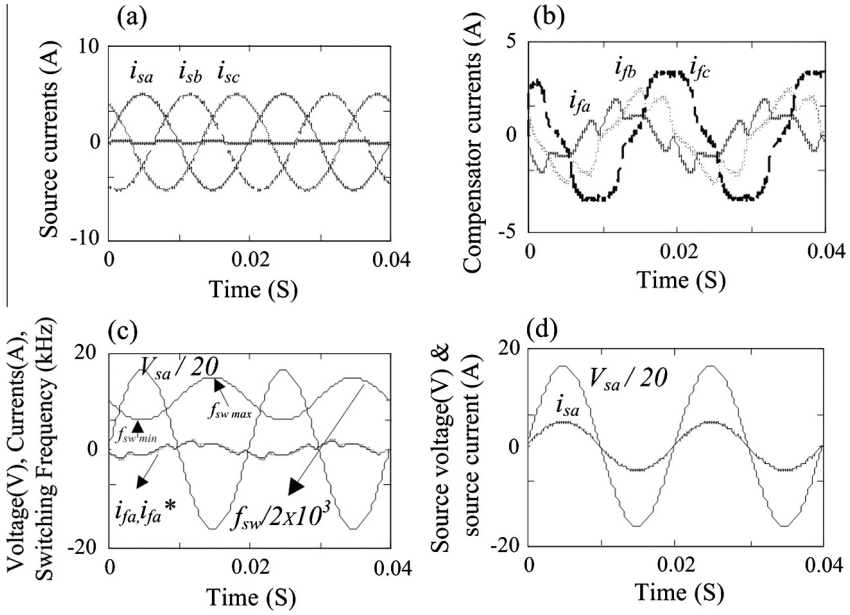

Fig. 10. Simulation results with Active NPC DSTATCOM (a) source currents (b) DSTATCOM injected currents (c) source voltage, injected current, reference current and switching frequency (d) source voltage and source currents (phase-a).

change in the compensator reference currents. When the analysis of the switching frequencies is done for all the above three NPC topologies, a slight variation in the minimum/maximum switching frequencies are found (Table 6), which is mainly because of the slight hysteresis band limit violation due to compensator currents. Finally, it is evident from Fig. 10(d) that this topology also provides UPF at the source side.

Lastly, Fig. 11 shows the balanced capacitor voltages for CNPC, MNPC and ANPC, which depicts the almost similar performance for all the three topologies, maintaining the capacitor voltages almost to their reference value (500 V).

Discussion

The performance evaluation of all the above DSTATCOM topologies is done extensively and presented in Table 6. From the analysis, it is to be noted that, all the topologies are able to provide balanced and sinusoidal source currents with almost zero neutral current and PF closed to unity. While, amongst all, the ANPC shows an adequately improved performance with source currents exactly equal to 3.48 A. As compared to CNPC and MNPC based compensators, the THD in source current is found to be reduced (less than 2%) and neutral current is observed to be reduced to 0.1493 A

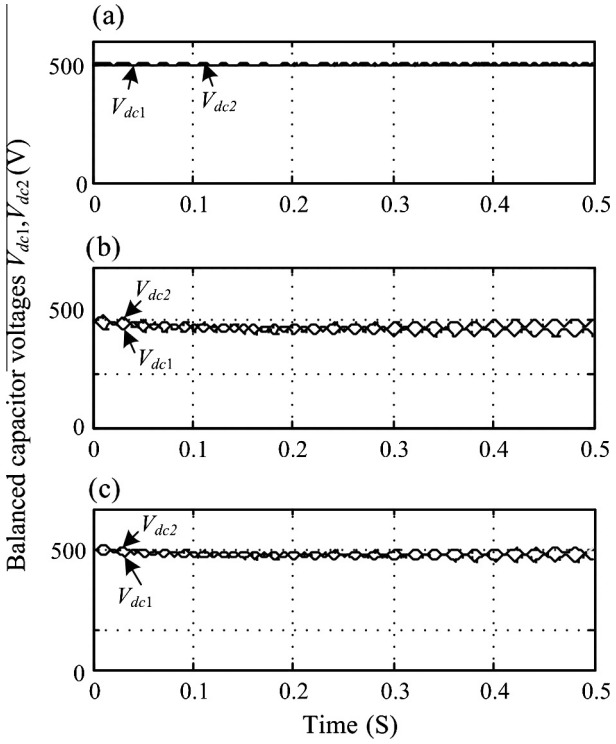

Fig. 11. Balanced capacitor voltages (a) CNPC (b) MNPC (c) ANPC.

(which is much less than both the topologies) in ANPC. Also, it is seen from the tabulated results that the average number of switching per cycle and switching frequency, for ANPC topology is less, which indicates, probably the low switching losses and improved efficiency. Further, it is seen that the compensator currents are slightly reduced, which indicate that, ANPC requires reduced DSTATCOM rating as compared to other topologies, to compensate the same amount of load. In the proposed topologies, the switching frequency is varying over a considerable wide range, which increases the stress level on the switches and the switching losses; thus reducing efficiency.

Conclusion

In this paper, MNPC and ANPC based new DSTATCOM topologies are proposed. Based on the simulation results, the effectiveness of different DSTATCOM topologies are focused and their comparative evaluation is presented. Unlike CNPC, the MNPC and ANPC topologies require no clamping diodes. In addition, more redundancy in ANPC allows the flexible switching strategies. ANPC shows marginal improvement in compensation compared to MNPC and CNPC along with satisfactory execution of hysteresis modulation scheme and ISCT control algorithm. From analysis, among proposed topologies, the ANPC seems to be better DSATCOM topology for load compensation.

References

[1] Ghosh A, Ledwich G. Power quality enhancement using custom power devices. London: Kluwer Academic Publishers; 2002.
[2] Mahmud MA, Pota HR, Hossain MJ. Nonlinear DSTATCOM controller design for distribution network with distributed generation to enhance voltage stability. Int J Electr Power Energy Syst 2013;53:974–9.
[3] Zaveri T, Bhalja BR, Zaveri N. Load compensation using DSTATCOM in three-phase, three-wire distribution system under various source voltage and delta connected load conditions. Int J Electr Power Energy Syst 2012; 41(1):34–43.
[4] Iyer S, Ghosh A, Joshi A. Inverter topologies for DSTATCOM applications-a simulation study. Elect Power Syst Res 2005;75(2–3):161–70.
[5] Gupta R, Ghosh A, Joshi A. Control of cascaded transformer multilevel inverter based DSTATCOM. Electr Power syst Res 2007;77(8):989–99.
[6] Shukla A, Ghosh A, Joshi A. Control scheme for dc capacitor voltage equalization in diode-clamped multilevel inverter based DSTATCOM. IEEE Trans Power Del 2008;23(2):1139–49.
[7] Srikanthan S, Mishra MK. DC capacitor voltage equalization in neutral point clamped inverter for DSTATCOM application. IEEE Trans Ind Electron 2010;57(8):2768–75.
[8] Nabae A, Takahashi I, Akagi H. A neutral-point-clamped PWM inverter. IEEE Trans Ind Appl 1981;17(5):518–23.
[9] Rodriguez J, Lai JS, Peng FZ. Multilevel inverters: a survey of topologies, control and applications. IEEE Trans Ind Electron 2002;49(4):724–38.
[10] Schweizer M, Lizama I, Friedli T, Kolar JW. Comparison of the chip area usage of 2-level and 3- level voltage source converter topologies. In: Proceedings of the 36th Annual IEEE industrial electronics society conference (IECON), vol. 1; November 2010. p. 391–96.
[11] Teodorescu R, Liserre M, Rodriguez P. Grid converters for photovoltaic and wind power systems. UK: A John Wiley Publishers; 2011.
[12] Barbosa P, Steimer P, Steinke J, Meysenc L, Winkelkemper M, Celanovic N. Active neutral-point-clamped multilevel converters. In: Proceedings of the 36th Annual IEEE power electronics specialists conference (PESC), vol. 1; June 2005. p. 2296–301.
[13] Bruckner T, Bernet S, Guldner H. The active NPC converter and its loss-balancing control. IEEE Trans Ind Electron 2005;52(3):855–68.
[14] Serpa LA, Pannaluri S, Barbosa PM, Kolar JW. A modified direct-power control strategy allowing the connection of three-phase inverter to the grid through LCL filters. IEEE Trans Ind Applic 2007;43(5):1388–400.
[15] Zare F, Ledwich G. A hysteresis current control for single-phase multilevel voltage source inverter: PLD implementation. IEEE Trans Power Electron 2002;17(5):731–8.
[16] Bode GH, Holmes DG. Implementation of three level hysteresis current control for a single phase voltage source inverter. In: Proceeding of the 31st Annual IEEE power electronics specialists conference (PESC), vol. 1; June 2000. p. 33–8.
[17] Gawande SP, Ramteke MR. Current controlled PWM for multilevel voltage-source inverters with variable and constant switching frequency regulation techniques: a review. J Power Electron (JPE) (KIPE-South Korea) 2014;14(2):302–14.
[18] Herrera RS, Salmeron P, Kim HS. Instantaneous reactive power theory applied to active power filter compensation: different approaches, assessment, and experimental results. IEEE Trans Ind Electron 2008;55(1):184–96.
[19] Marques GD. A comparison of active filter control methods in unbalanced and non-sinusoidal conditions. In: Proceedings of 24th Annual IEEE industrial electronics society conference (IECON), vol. 1; August 1998. p. 444–49.
[20] Zaveri T, Bhalja BR, Zaveri N. Comparison of control strategies for DSTATCOM in three-phase, four-wire distribution system for power quality improvement under various source voltage and load conditions. Int J Electr Power Energy Syst 2012;43(1):582–94.
[21] Luo A, Fang L, Xu X, Peng S, Wu C, Fang H. New control strategy for DSTATCOM without current sensors and its engineering application. Int J Electr Power Energy Syst 2011;33(2):322–31.
[22] Ghosh A, Joshi A. A new approach to load balancing and power factor correction in power distribution system. IEEE Trans Power Del 2000;15(1):417–22.
[23] Jouanne AV, Dai S, Zhang H. A multilevel inverter approach providing dc-link balancing, ride-through enhancement, and common-mode voltage elimination. IEEE Trans Ind Electron 2002;49(4):739–45.
[24] Mishra MK, Ghosh A, Joshi A. Control strategies for capacitor voltage equalization in neutral clamped shunt compensation. In: Proceeding of IEEE power engineering society winter meeting (PES), vol. 1; January 2001. p. 132–37.
[25] Mishra MK, Karthikeyan K. An investigation of design and switching dynamics of a voltage source inverter to compensate unbalanced and nonlinear. IEEE Trans Ind Electron 2009;56(8):2802–10.