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Voltage-boosting converters with hybrid energy pumping

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Abstract: Voltage-boosting converters with hybrid energy pumping are presented. Hence, the corresponding voltage conversion ratios are higher than the traditional boost converter or some existing voltage-boosting converters. Above all, by changing the circuit connection or turn-on types of switches, there are three voltage conversion ratios to be generated. Hence, there are three types of voltage-boosting converters to be presented herein. Furthermore, for any type, no isolated gate driver is needed instead of one half-bridge gate driver and one low-side gate driver, and the voltage stress on the low-side switch to magnetise the inductor and the voltage stress on the output diode can be reduced as compared to the traditional boost converter. In addition, the basic operating principles of these converters are easy to describe and analyse along with mathematical deductions.

1 Introduction

For the applications of the power supply using the low-voltage battery, analogue circuits, such as radio frequency (RF) amplifier, audio amplifier, and so on, often need high voltage to obtain enough output power and voltage amplitude. This is achieved by boosting the low voltage to the required high voltage [1–3]. For the traditional boost converter, it pumps the energy stored in the inductor plus the input voltage into the output during the turn-off period of the switch driven from the pulse-width modulation (PWM) control signal created from the controller, whereas for the KY converter [4], it pumps the energy stored in the capacitor plus the input voltage into the output during the turn-on period of the switch driven from the PWM control signal created from the controller. In [4], in order to increase the voltage conversion ratio of the KY converter, another one charge pump cell is added to the KY converter, and hence two converters, called second-order-derived KY converters, are created due to different PWM control strategies. However, the corresponding voltage conversion ratios mentioned in [4] are limited to some extent. Consequently, in [5–15], there have been some voltage-boosting converters presented. In [5–8], high voltage conversion ratios are achieved via coupling inductors or transformers, but the voltage spikes due to the accompanying leakage inductances and the complexity in the corresponding circuit analysis are unavoidable. In [9], a floating output, together with a complicated circuit, makes application and analysis not so easy. In [10], although such a converter is simple in structure, its output is floating, thereby limiting its applications to some extent. Furthermore, there is one switch needing isolated driving. In addition, the voltage conversion ratio of this converter is $(1 + D)/(1 - D)$, which is lower than any one of voltage conversion ratios of the proposed converters. In [11], there are two converters presented, and the voltage conversion ratio of each converter can be increased by increasing the number of voltage multiplier cells. The voltage conversion ratios for these two converters are the same and equal to $(M + 1)/(1 - D)$, where M is the number of multiplier stages. The components used in the main power stages for these two converters with M equal to one are almost the same as those for the proposed converters. Although the voltage conversion ratios for these two converters are the same as that for one of the proposed converters, the operating analyses for these two converters are more complex than that for any one of the proposed converters. In [12], although this converter possesses the voltage conversion ratio of $1/(1 - D)^2$, its control-to-output transfer function has three zeros in the half-right plane, and hence high stability and good closed-loop performance are very difficult to achieve. This is because the phase margin is severely degraded by these zeros. In [13], a cascaded boost converter is presented with one active clamp circuit added to reduce the voltage stresses on the switch and diode, along with zero current switching considered. By doing so, the circuit complexity is increased. In addition, this converter has high non-linearity in voltage conversion ratio of $1/(1 - D)^2$, and this renders the overall system not easy to control. In [14], although this voltage-boosting converter possesses a simple operating principle, its voltage conversion ratio is limited to some extent. In [15], although this circuit has a high voltage conversion ratio, the high non-linearity in voltage conversion ratio against duty cycle causes the overall system not to be easy to control. Moreover, there is one switch needing isolated driving.

Based on the aforementioned analysis, simple voltage-boosting converters with hybrid energy pumping are presented herein. Any one of the proposed converters described in this paper pumps the energy stored in the capacitor and inductor plus the input voltage into the output during the turn-off period of the switch driven from the PWM control signal created from the controller, so as to increase the voltage conversion ratios. Hence, three types of converters are to be addressed in this paper based on the circuit structure and the PWM control strategy. Hence, the corresponding voltage conversion ratios are no less than that for the traditional boost converter or any other converter shown in [4, 10, 11]. Furthermore, the voltage stress on the low-side switch to magnetise the inductor and the voltage stress on the output diode can be decreased as compared to the traditional boost converter. Above all, by changing circuit connection or changing the turn-on types of switches, there are three voltage conversion ratios to be yielded. That is, there are three types of voltage-boosting converters to be addressed herein. In addition, no isolated gate driver is needed instead of one half-bridge gate driver and one low-side gate driver. The detailed illustration of the basic operating principles of such converters is given, along with some experimental results offered to demonstrate the effectiveness of the proposed topologies.

2 Proposed converter topologies

In this paper, there are three types of voltage conversion ratios in the proposed two voltage-boosting converter structures. Hence, the type 1 converter is described on the left of Fig. 1*a*, whereas the types 2 and 3 converters are illustrated on the right of Fig. 1*a* with different PWM control strategies. That is, these three converters are obtained via different positions of the anode of D_{b2} and different PWM control strategies. Each converter contains three metal-oxide semiconductor field-effect transistor (MOSFET) switches S_1, S_2 and S_3 along with three body diodes D_1, D_2 and D_3, two energy-transferring capacitors C_{b1} and C_{b2} which are large enough to keep the voltages across themselves constant at some values, two charge pump diodes D_{b1} and D_{b2}, one output diode D_o, one inductor L inserted between C_{b1} and C_{b2}, one output capacitor C_o and one output resistor R_o.

3 Basic operating principles

Before this section is taken up, there are some assumptions given as follows: (i) the blanking times between the switches are omitted; (ii) the voltage drops across the switches and diodes during the turn-on period are negligible; (iii) since the energy-transferring capacitors C_{b1} and C_{b2}, operating based on the charge pump principle, are abruptly charged to some voltage within a very short time, which is much less than the switching period T_s, the values of C_{b1} and C_{b2} are large enough to keep the voltages across themselves constant at some values, and it is reasonable that the voltages across the capacitors C_{b1} and C_{b2} are v_i and $2v_i$ for type 1, respectively, and the voltages across the capacitors C_{b1} and C_{b2} are both v_i for types 2 and 3; (iv) the input voltage is signified by v_i, the input current is expressed by i_i, the output voltage is represented by v_o, and the currents flowing through L, C_{b1} and C_{b2} are denoted by i_L, i_{b1} and i_{b2}, respectively; and (v) for analysis convenience, these three converters operate in the continuous conduction mode (CCM) and hence there are only two operating modes for each converter.

For these three converters to be considered, the turn-on types of the three switches are described in Table 1, where D is the duty cycle of the PWM control signal created from the controller. For any type of these converters, the following analyses contain the explanation of the power flow direction in each mode, the description of the corresponding differential equations, the resulting relationship between the DC input and output voltages and the accompanying small-signal AC models.

3.1 Type 1 converter

3.1.1 Mode 1: As shown on the left of Fig. 1*b*, S_1 and S_3 are turned on, but S_2 is turned off. Owing to S_3 being turned on, D_o is reverse-biased and D_{b2} is forward-biased, thereby causing C_{b2} to be abruptly charged to $2v_i$ within a very short time, whereas due to S_1 being turned on, D_{b1} is reverse-biased, thereby causing C_{b1} to be discharged. At the same time, the voltage across L is $2v_i$, thereby causing L to be magnetised. Also, C_o releases energy to the output. Therefore the corresponding differential equations are

$$\begin{cases} L\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = 2v_i \\ C_o\dfrac{\mathrm{d}v_o}{\mathrm{d}t} = \dfrac{-v_o}{R_o} \\ i_i = i_L + i_{b2} \end{cases} \tag{1}$$

3.1.2 Mode 2: As shown on the right of Fig. 1*b*, S_1 and S_3 are turned off, but S_2 is turned on. Owing to S_2 being turned on, D_{b1} is forward-biased, thereby causing C_{b1} to be abruptly charged to v_i within a very short time, whereas due to S_3 being turned off, D_o is forward-biased, thereby causing C_{b2} to be discharged. At the same time, the voltage across L is $3v_i - v_o$, thereby causing L to be demagnetised and D_{b2} to be reverse-biased. Also, C_o is energised. Hence, the accompanying differential equations are

$$\begin{cases} L\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = 3v_i - v_o \\ C_o\dfrac{\mathrm{d}v_o}{\mathrm{d}t} = i_L - \dfrac{v_o}{R_o} \\ i_i = i_L + i_{b1} \end{cases} \tag{2}$$

According to (1) and (2), and the voltage-second balance, the DC voltage conversion ratio of this converter, M, can be represented as

$$M = \frac{V_o}{V_i} = \frac{3-D}{1-D} \tag{3}$$

where V_o and V_i are the DC parts of v_o and v_i, respectively.

3.2 Type 2 converter

3.2.1 Mode 1: As shown on the left of Fig. 1*c*, S_1 and S_3 are turned on, but S_2 is turned off. Owing to S_3 being turned on, D_{b2} is forward-biased, thereby causing C_{b2} to be abruptly charged to v_i within a very short time, whereas due to S_1

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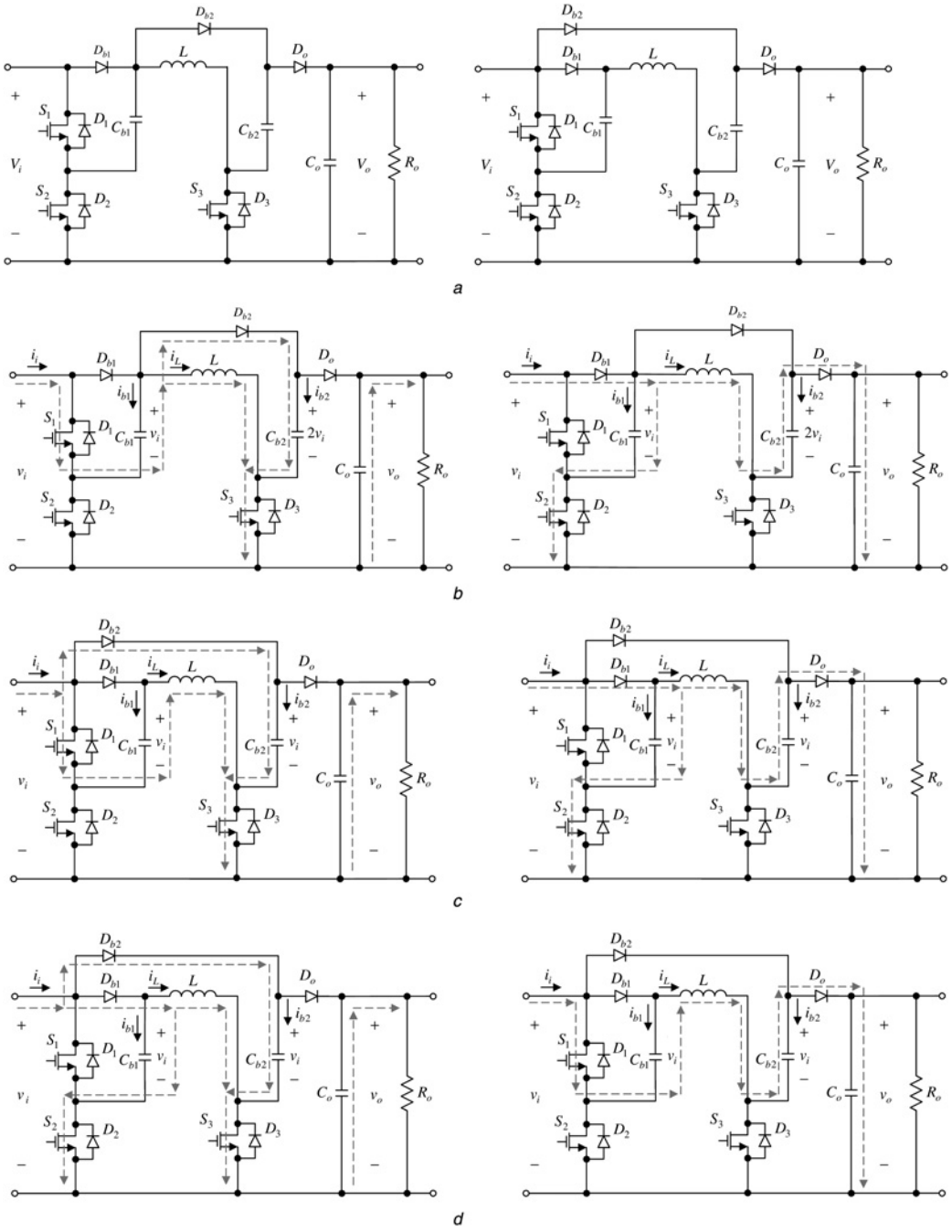

Fig. 1 *Proposed converters and their basic operating principles of the proposed converters*

a Type 1 on the left, types 2 and 3 on the right
b Power flow of type 1 in mode 1 on the left and power flow of type 1 in mode 2 on the right
c Power flow of type 2 in mode 1 on the left and power flow of type 2 in mode 2 on the right
d Power flow of type 3 in mode 1 on the left and power flow of type 3 in mode 2 on the right

Table 1 Turn-on types of switches

Type	S_1	S_2	S_3
type 1	D	$1-D$	D
type 2	D	$1-D$	D
type 3	$1-D$	D	D

being turned on, D_{b1} is reverse-biased, thereby causing C_{b1} to be discharged. At the same time, the voltage across L is $2v_i$, thereby causing L to be magnetised. Also, C_o releases energy to the output. Hence, the corresponding differential equations are

$$\begin{cases} L\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = 2v_\mathrm{i} \\ C_\mathrm{o}\dfrac{\mathrm{d}v_\mathrm{o}}{\mathrm{d}t} = \dfrac{-v_\mathrm{o}}{R_\mathrm{o}} \\ i_\mathrm{i} = i_L + i_{b2} \end{cases} \tag{4}$$

3.2.2 Mode 2: As shown on the right of Fig. 1*c*, S_2 is turned on, but S_1 and S_3 are turned off. Owing to S_2 being turned on, D_{b1} is forward-biased, thereby causing C_{b1} to

be abruptly charged to v_i within a very short time, whereas due to S_3 being turned off, D_{b2} is reverse-biased, thereby causing C_{b2} to be discharged. At the same time, the voltage across L is $2v_i - v_o$, thereby causing L to be demagnetised. Also, C_o is energised. Hence, the resulting differential equations are

$$\begin{cases} L\dfrac{di_L}{dt} = 2v_i - v_o \\ C_o\dfrac{dv_o}{dt} = i_L - \dfrac{v_o}{R_o} \\ i_i = i_L + i_{b1} \end{cases} \quad (5)$$

According to (4) and (5), the DC voltage conversion ratio of this converter, M, can be represented by

$$M = \frac{V_o}{V_i} = \frac{2}{1-D} \quad (6)$$

3.3 Type 3 converter

3.3.1 Mode 1: As shown on the left of Fig. 1*d*, S_2 and S_3 are turned on, but S_1 is turned off. Owing to S_2 and S_3 being turned on, D_{b1} and D_{b2} are forward-biased, thereby causing C_{b1} and C_{b2} to be abruptly charged to v_i within a very short time. At the same time, the voltage across L is v_i, thereby causing L to be magnetised. Also, C_o releases energy to the

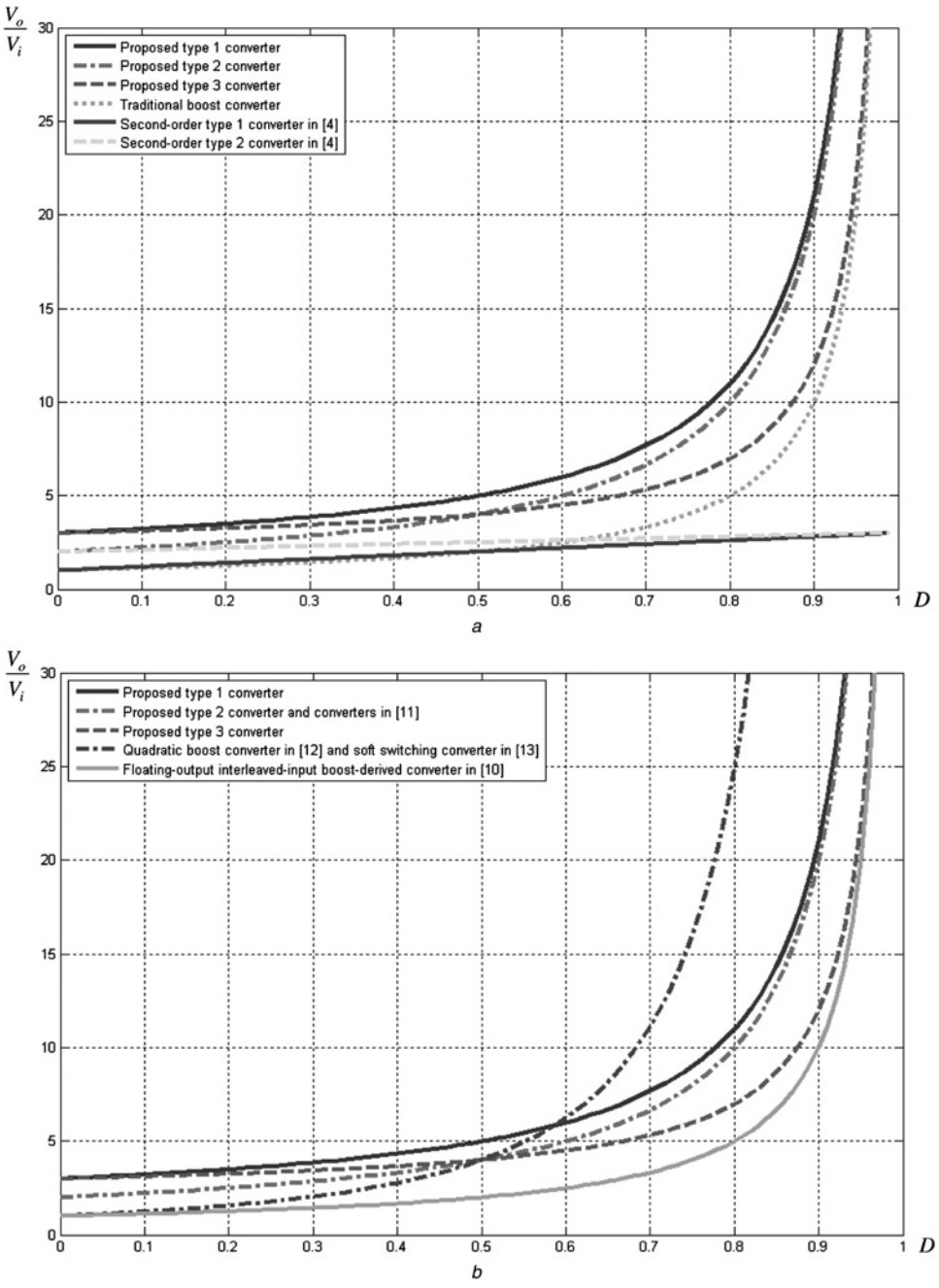

Fig. 2 *Curves of voltage conversion ratio against duty cycle*

a Proposed converters, the traditional boost converter and the converters in [4]
b Proposed converters and the converters in [10–13]

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output. Hence, the corresponding differential equations are

$$\begin{cases} L\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = v_\mathrm{i} \\ C_\mathrm{o}\dfrac{\mathrm{d}v_\mathrm{o}}{\mathrm{d}t} = \dfrac{-v_\mathrm{o}}{R_\mathrm{o}} \\ i_\mathrm{i} = i_L + i_{b1} + i_{b2} \end{cases} \tag{7}$$

3.3.2 Mode 2: As shown on the right of Fig. 1*d*, S_2 and S_3 are turned off, but S_1 is turned on. Owing to S_1 being turned on, D_{b1} is reverse-biased, thereby causing C_{b1} to be discharged, whereas due to S_3 being turned off, D_o is forward-biased, thereby causing C_{b2} to be discharged. At the same time, the voltage across L is $3v_\mathrm{i} - v_\mathrm{o}$, thereby causing L to be demagnetised and D_{b2} to be

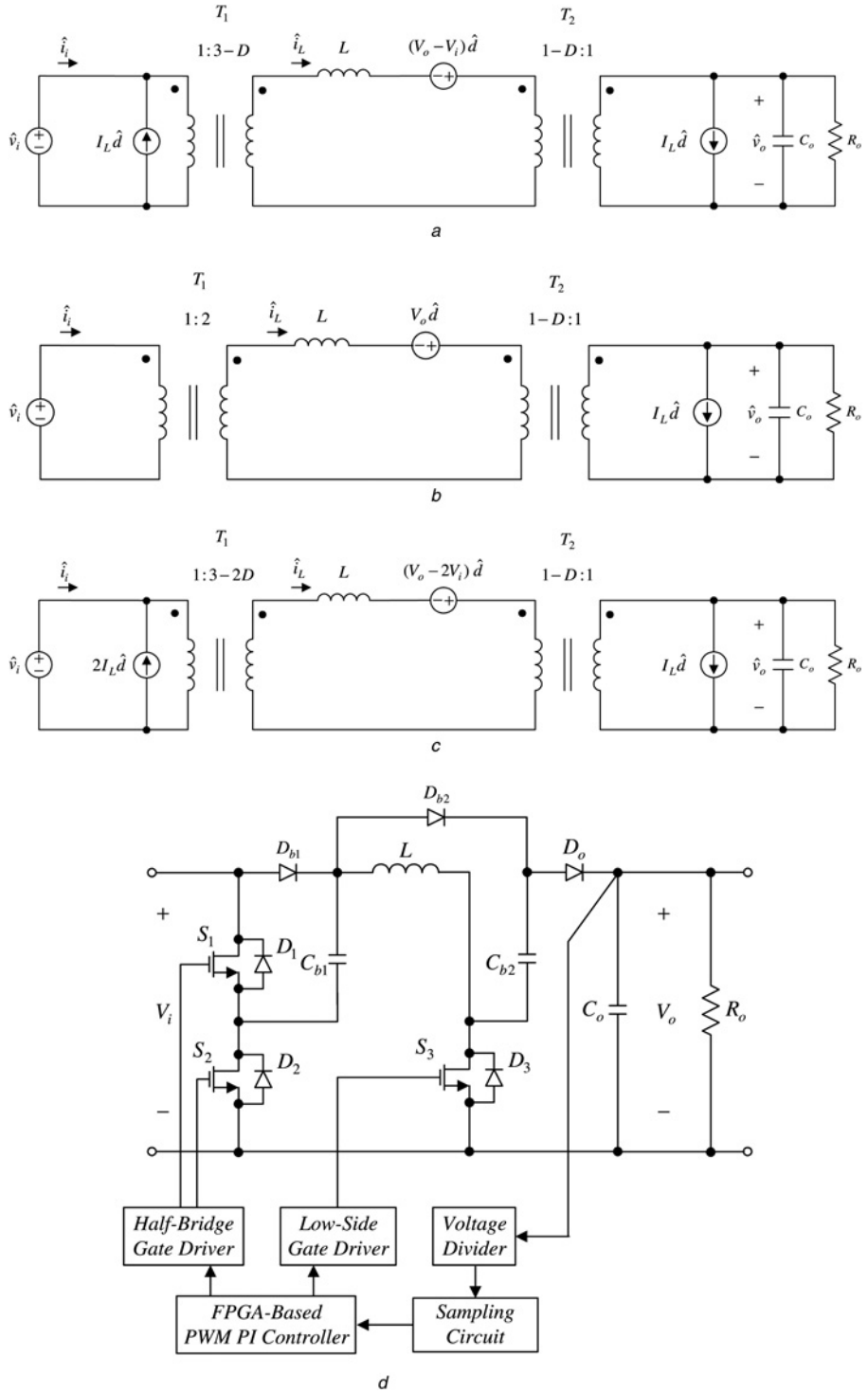

Fig. 3 *Small-signal AC models of the proposed converters and overall system block diagram*

a Type 1
b Type 2
c Type 3
d Overall system block diagram for type 1

reverse-biased. Also, C_o is energised. Therefore the resulting differential equations are

$$\begin{cases} L\dfrac{di_L}{dt} = 3v_i - v_o \\ C_o\dfrac{dv_o}{dt} = i_L - \dfrac{v_o}{R_o} \\ i_i = i_L = i_{b1} = i_{b2} \end{cases} \quad (8)$$

According to (7) and (8), the DC voltage conversion ratio of this converter, M, can be represented to be

$$M = \frac{V_o}{V_i} = \frac{3-2D}{1-D} \quad (9)$$

From the aforementioned analysis, three types of voltage-boosting converters have individual voltage conversion ratios. Fig. 2*a* shows the curves of voltage conversion ratio against duty cycle for the proposed converters, the traditional boost converter and the second-order-derived KY converters [4]. From Fig. 2*a*, it can be seen that the proposed converters have higher voltage conversion ratios than the traditional boost converter and the second-order-derived KY converters. Further, to do comparisons between the proposed converters and the converters in [10–13], from Fig. 2*b*, it can be seen that the voltage conversion ratio in [10] is the smallest among them. Furthermore, the voltage conversion ratio in [11] is smaller than that of the proposed type 1 converter, the same as that of the proposed type 2 converter, smaller than that of the proposed type 3 converter if the duty cycle is smaller than 0.5 and larger than that of the proposed type 3 converter if the duty cycle is larger than 0.5. On the other hand, in [12, 13], both the voltage conversion ratios are $1/(1-D)^2$, which is the largest among those for the proposed converters and the converters in [10, 11] as the duty cycle is larger than 0.6. However, such a voltage conversion ratio possesses high non-linearity, thereby making the overall systems in [12, 13] not easy to control.

3.4 Small-signal AC models

According to [1], the small-signal AC models for the proposed three converters can be obtained, which are sketched in Figs. 3*a–c*, where a variable x denotes voltage or current or duty cycle, X represents the DC value of x, and $\hat{x}$ indicates the variation in x. Based on these models, the corresponding control-to-output transfer functions can be attained.

For type 1

$$G_{vd1}(s) = \frac{((V_o - V_i)/(1-D))[1-(sLI_L/(V_o - V_i)(1-D))]}{s^2(LC_o/(1-D)^2) + s(L/R_o(1-D)^2) + 1} \quad (10)$$

For type 2

$$G_{vd2}(s) = \frac{(V_o/1-D)[1-(sLI_L/V_o(1-D))]}{s^2(LC_o/(1-D)^2) + s(L/R_o(1-D)^2) + 1} \quad (11)$$

For type 3

$$G_{vd3}(s) = \frac{((V_o - 2V_i)/(1-D))[1-(sLI_L/(V_o - 2V_i)(1-D))]}{s^2(LC_o/(1-D)^2) + s(L/R_o(1-D)^2) + 1} \quad (12)$$

3.5 Semiconductor stresses

The steady-state voltage and current stresses on the semiconductors of the proposed converters except the body diodes of MOSFET switches are tabulated in Table 2, on the assumption that the voltages across switches and diodes during the turn-on interval are negligible and the voltages across C_{b1} and C_{b2} are V_i and $2V_i$ for type 1, respectively, and the voltages across the capacitors C_{b1} and C_{b2} are both V_i for types 2 and 3. As for Table 3, it gives the stress values for semiconductors with voltage conversion ratios obtained from the beginning of Section 5. In Table 2, the symbols from a to f have the following meanings.

1. a: V_i.
2. b: $2V_i$.
3. c: $V_o - V_i$.
4. d: $V_o - 2V_i$.
5. e: V_o.
6. f: $P_{o\text{-rated}}/(V_o(1-D)) + I_{o\text{-min}}/(1-D)$.

As generally acknowledged, the voltages across the switch and output diode of the traditional boost converter are equal to the output voltage. But from Tables 2 and 3, it can be seen that for any type, the voltage across the switch S_3 and the voltage across the output diode D_o are smaller than those for the traditional boost converter, respectively.

Table 2 Semiconductor stresses

	S_1	S_2	S_3	D_{b1}	D_{b2}	D_o
for type 1						
voltage stress (V)	*a*	*a*	*d*	*a*	*c*	*d*
current stress (A)	*f*	0	*f*	*f*	0	*f*
for type 2						
voltage stress (V)	*a*	*a*	*c*	*a*	*c*	*c*
current stress (A)	*f*	0	*f*	*f*	0	*f*
for type 3						
voltage stress (V)	*a*	*a*	*c*	*a*	*c*	*c*
current stress (A)	*f*	0	*f*	*f*	0	*f*

Table 3 Semiconductor stress values

	S_1	S_2	S_3	D_{b1}	D_{b2}	D_o
for type 1 with $M = 1/2$						
voltage stress (V)	12	12	36	12	48	36
current stress (A)	1.47	0	1.47	1.47	0	1.47
for type 2 with $M = 3/5$						
voltage stress (V)	12	12	48	12	48	48
current stress (A)	1.83	0	1.83	1.83	0	1.83
for type 3 with $M = 2/3$						
voltage stress (V)	12	12	48	12	48	48
current stress (A)	2.2	0	2.2	2.2	0	2.2

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4 Control method applied

Fig. 3*d* shows the overall system block diagram for type 1, where the field programmable gate array (FPGA)-based PWM control strategy based on the one-comparator counter-based sampling [16] is employed herein. The output voltage information after the voltage divider is obtained through the sampling circuit, and then sent to FPGA having a system clock of 100 MHz to create the desired PWM control signals to drive the MOSFET switches after the gate drivers. As for types 2 and 3, they adopt the same control methods as type 1.

By substituting the parameter values into (10) to (12), the proportional–integral (PI) controller parameters, the proportional gain k_p and the integral gain k_i can be obtained based on MATLAB/SISOTOOL under the condition that the crossover frequency is smaller than ten times of the switching frequency, the gain margin is larger than 6 dB and the phase margin is larger than 45°. However, in practice, owing to the parasitic and non-ideal components in the circuit, the values of k_p and k_i are finally set at 0.02 and 0.04 for type 1, respectively, 0.025 and 0.03 for type 2, respectively, and 0.018 and 0.03 for type 3, respectively.

5 Key parameter considerations

Before this section is discussed, there are some specifications and assumptions to be given as follows: (i) the rated DC input voltage V_i is set to 12 V; (ii) the rated DC output voltage V_o is set to 60 V; (iii) the rated DC output power $P_{o\text{-}rated}$ is set to 40 W; (iv) the input power is equal to the output power for any load; (v) the converters are designed to operate in CCM above the minimum output power $P_{o\text{-}min}$ of 4 W, which is 10% of $P_{o\text{-}rated}$; (vi) the switching frequency f_s is chosen to be 195 kHz; (vii) one 680 μF electrolytic capacitor is chosen for C_o; (viii) the product names of D_{b1}, D_{b2} and D_o are MBR3045PT, MBR40100PT and MBR40100PT, respectively; (ix) the product names of S_1, S_2 and S_3 are

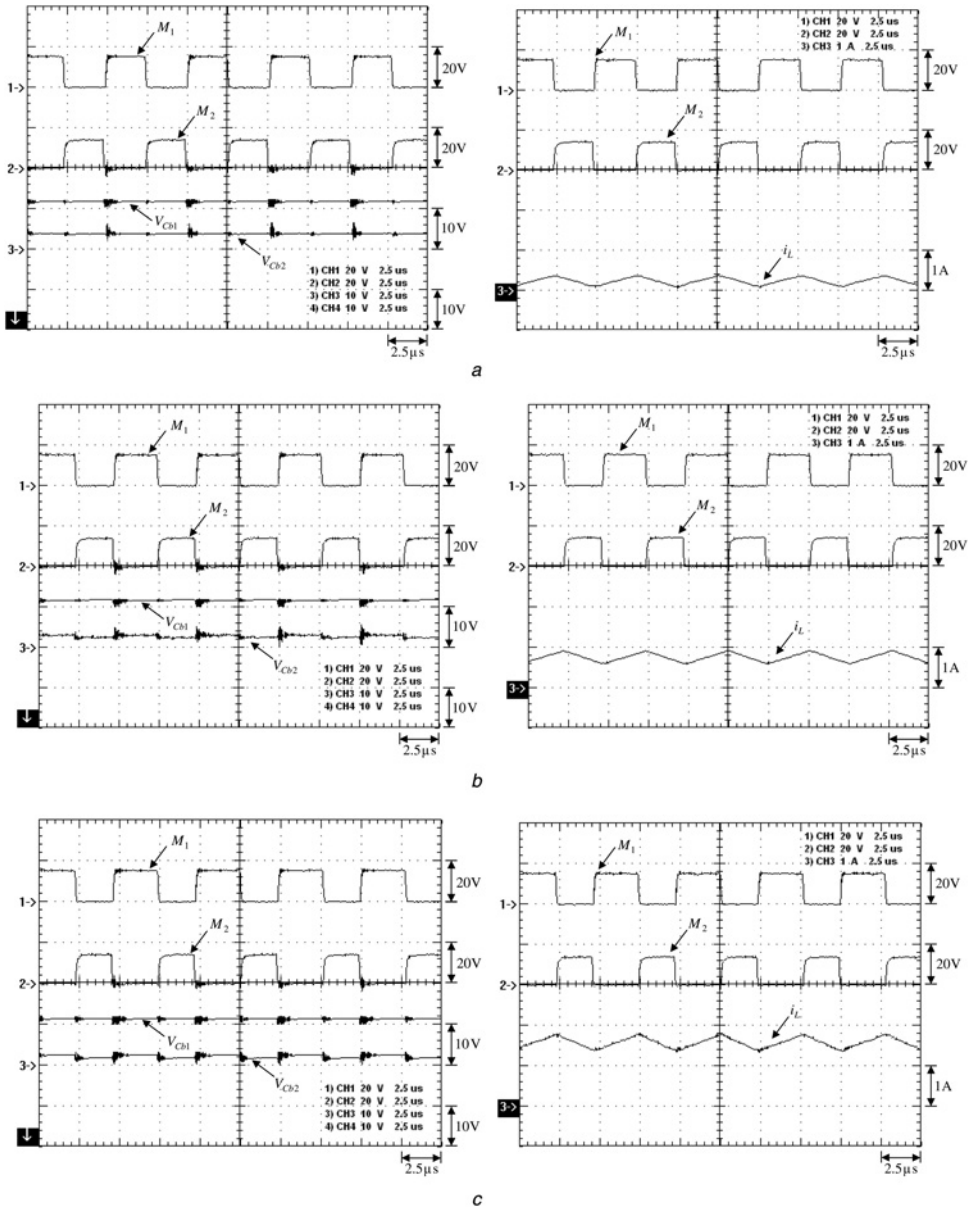

Fig. 4 *Experimental waveforms for type 1*

a, *b* and *c* under 10, 50 and 100% of the rated load, respectively – (1) M_1; (2) M_2; (3) V_{Cb1}; (4) V_{Cb2} on the left; (1) M_1; (2) M_2; (3) i_L on the right

FDMC7672S, FDMC7672S and FDP120N10, respectively; (x) the product name of FPGA is EP1C3T100C8; (xi) the product name of the comparator is LT1719; (xii) the product name of the half-bridge gate driver is IR2011 and (xiii) the product name of the low-side gate driver is MIC4420.

5.1 Design of energy-transferring capacitors

The values of the energy-transferring capacitors C_{b1} and C_{b2} play important roles in the proposed converters. So, the following focuses on how to design C_{b1} and C_{b2} so as to make sure that the voltages across themselves are kept as constant as possible at some values. There are some assumptions used to obtain the values of C_{b1} and C_{b2} as follows: (i) the peak-to-peak value of the voltage ripple is set to 0.1% of the DC voltage across itself for each capacitor; and (ii) the input voltage is an infinite bus, that is, the input voltage is kept constant and can be represented as infinite capacitance, which is much larger than the values of C_{b1} and C_{b2}.

For type 1, C_{b1} and C_{b2} are abruptly charged to V_i and $2V_i$, respectively. Hence, the values of C_{b1} and C_{b2} can be obtained based on the varied charge equal to the capacitance multiplied by the varied voltage, and the corresponding equations are

$$\Delta v_{Cb1} = \frac{1}{C_{b1}} \int_0^{DT_s} i_{b1} \mathrm{d}t \tag{13}$$

$$\Delta v_{Cb2} = \frac{1}{C_{b2}} \int_0^{(1-D)T_s} i_{b2} \mathrm{d}t \tag{14}$$

where T_s is the switching period, and Δv_{Cb1} is the variation in the voltage across C_{b1} discharged during the turn-on period whereas Δv_{Cb2} is the variation in the voltage across C_{b2} discharged during the turn-off period.

Therefore, according to (13) and (14) and the aforementioned assumptions, the values of C_{b1} and C_{b2} can be worked out to be 145 and 285 μF, respectively, and finally are set at 220 and 330 μF, respectively.

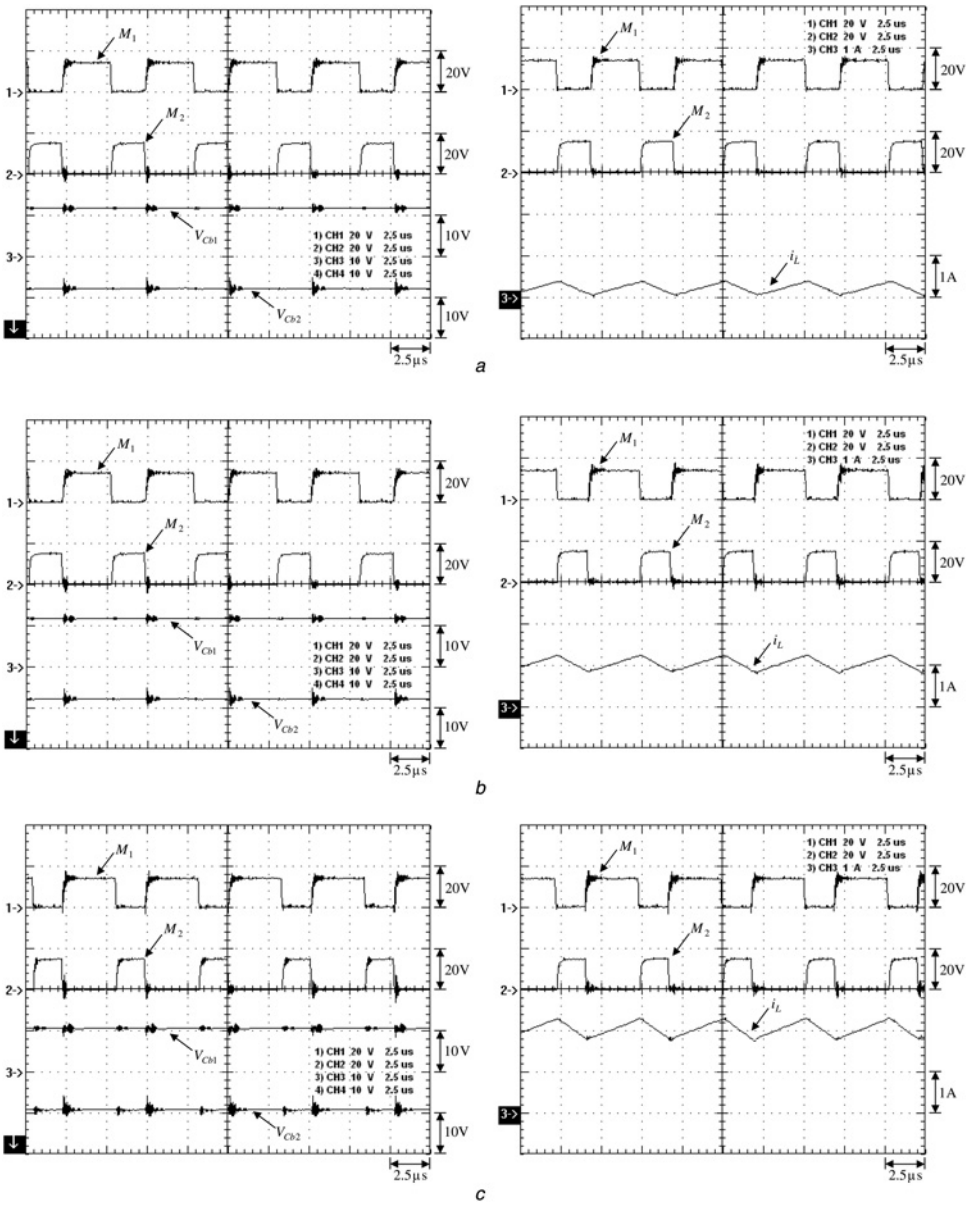

Fig. 5 *Experimental waveforms for type 2*

a, *b* and *c* Under 10, 50 and 100% of the rated load, respectively – (1) M_1; (2) M_2; (3) V_{Cb1}; (4) V_{Cb2} on the left; (1) M_1; (2) M_2; (3) i_L on the right

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On the other hand, for types 2 and 3, C_{b1} and C_{b2} are both abruptly charged to V_i, respectively. Therefore, based on the similar way mentioned in type 1, the values of C_{b1} and C_{b2} for type 2 can be figured out to be 427 and 285 μF, respectively, and eventually are set at 470 and 330 μF, respectively, whereas the values of both C_{b1} and C_{b2} for type 3 can be worked out to be 285 μF, and finally both are set at 330 μF.

5.2 Design of inductors

The inductance design is under the condition that the converter operates in CCM above the minimum output $P_{\text{o-min}}$. The inequality of type 1 for L can be expressed to be

$$L \geq \frac{V_i^2 D(3-D)T_s}{P_{\text{o-min}}} \tag{15}$$

According to the given specifications and (15), the value of L is calculated to be larger than 231 μH, and eventually is set at 235 μH.

The inequality of type 2 for L can be expressed to be

$$L \geq \frac{2V_i^2 DT_s}{P_{\text{o-min}}} \tag{16}$$

According to the given specifications and (16), the value of L is calculated to be larger than 221 μH, and eventually is set at 225 μH.

The inequality of type 3 for L can be expressed to be

$$L \geq \frac{V_i^2 D(3-2D)T_s}{2P_{\text{o-min}}} \tag{17}$$

According to the given specifications and (17), the value of L is calculated to be larger than 103 μH, and finally is set at 105 μH.

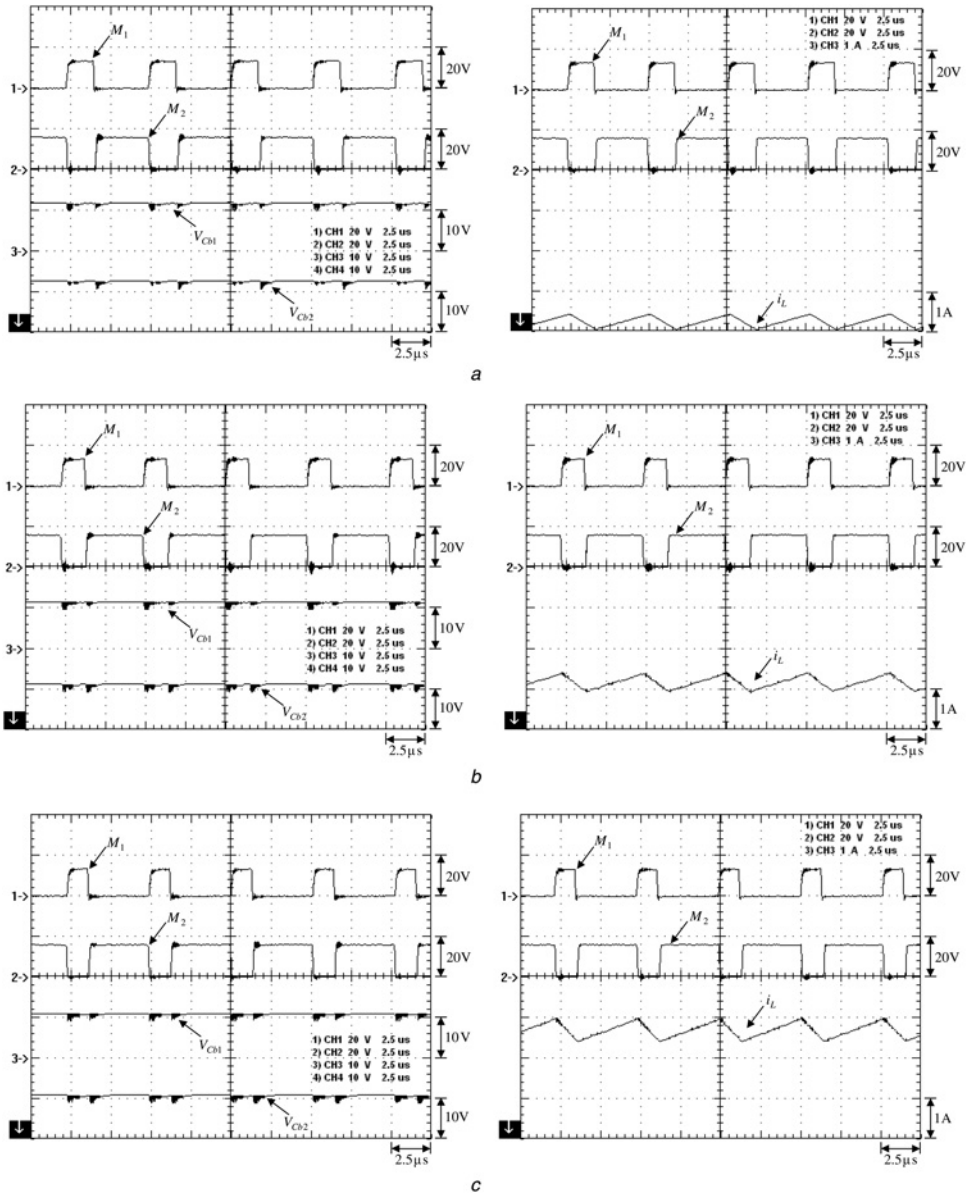

Fig. 6 *Experimental waveforms for type 3*

a, *b* and *c* Under 10, 50 and 100% of the rated load, respectively – (1) M_1; (2) M_2; (3) V_{Cb1}; (4) V_{Cb2} on the left; (1) M_1; (2) M_2; (3) i_L on the right

6 Experimental results

For a given converter, based on the one-comparator counter-based PWM control strategy using the FPGA, the parameters of the voltage-loop controller for all the associated experiments are the same. It is noted that the control efforts created from the individual PI controllers are used to generate PWM gate driving signals, M_1 for type 1, M_1 for type 2 and M_2 for type 3.

Figs. 4–6 are provided to verify the performances for types 1 to 3, respectively. All of the waveforms on the left of Figs. 4–6 depict the PWM gate driving signals M_1 and M_2 for S_1 and S_2, respectively, and the voltages V_{Cb1} and V_{Cb2} on C_{b1} and C_{b2}, respectively, under 10, 50 and 100% of the rated load. From these figures, it can be seen that V_{Cb1} and V_{Cb2} are kept constant in the vicinity of V_i and $2V_i$ for type 1, respectively, and both kept constant in the neighbourhood of V_i for types 2 and 3, respectively. It is noted that the more the load is, the lower the voltages on C_{b1} and C_{b2}. This is because the forward voltage drops and the voltages on the parasitic components are increased as the load current is increased. All of the waveforms on the right of Figs. 4–6 show the PWM gate driving signals M_1 and M_2 for S_1 and S_2, respectively, the current i_L in L, under 10, 50 and 100% of the rated load. It is noted that all the converters under 10% of rated load operate in CCM, and this corresponds to the design specifications. According to the aforementioned results, it is evident that the proposed voltage-boosting converters can stably operate under closed-loop control.

On the other hand, Fig. 7 is used to demonstrate the transient-state performances for types 1 to 3 respectively, without changing the controller parameters shown in Section 4. All of the waveforms on the left of Fig. 7 depict the load transient responses due to the load change from 50 to 100% of the rated load for types 1 to 3, respectively, whereas all of the waveforms on the right of Fig. 7 show the load transient responses due to the load change from

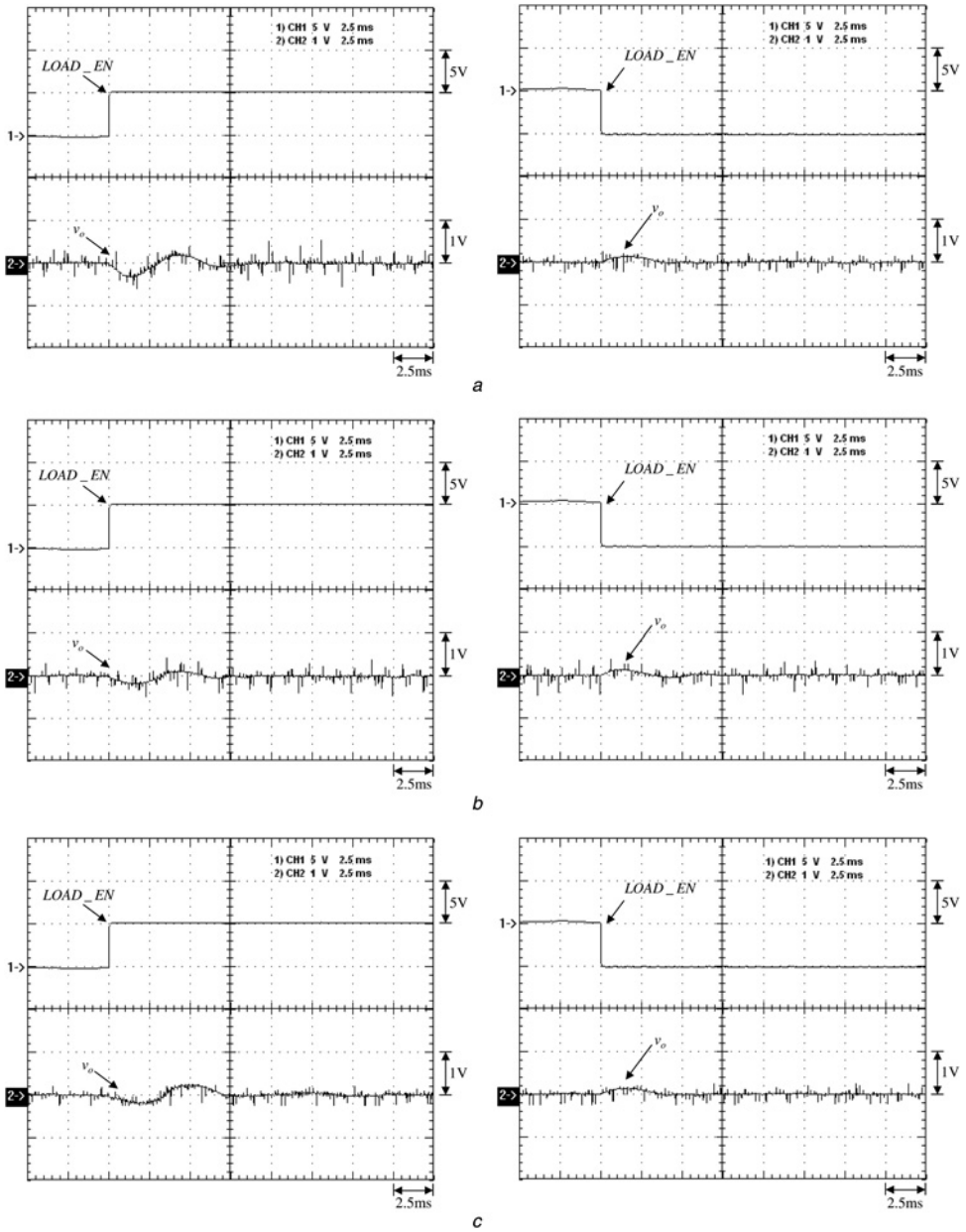

Fig. 7 *Load transient responses*

a, *b* and *c* For types 1, 2 and 3, respectively – due to load change from 50 to 100% load on the left; due to load change from 100 to 50% load on the right

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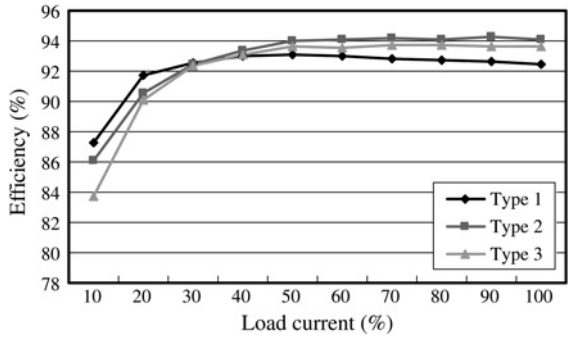

Fig. 8 *Curves of efficiency against load current for types 1, 2 and 3*

100 to 50% of the rated load for types 1 to 3, respectively. From these figures, it can be seen that for any type of converters, the peak-to-peak value of output voltage oscillation due to upload is within 1% of the rated DC output voltage and the corresponding recovery time is within 7.5 ms, whereas the peak-to-peak value of output voltage oscillation due to download is within 0.5% of the rated DC output voltage and the resulting recovery time is within 3.75 ms. Based on the aforementioned results, it is obvious that the proposed voltage-boosting converters have good transient-state performances.

Fig. 8 shows the curves of efficiency against load current for three types of voltage-boosting converters. From Fig. 8, it can be seen that all the proposed converters have the efficiencies above 83% at minimum load and above 92% at rated load. From the aforementioned experimental results, it can be seen that all these converters have good performances on stability and efficiency to some reasonable extent. Furthermore, under the same system specifications given in this paper, the duty cycle of type 2 lies between type 1 and type 3, and this can be seen in Table 3.

7 Conclusions

In this paper, three types of voltage-boosting converters, depending on circuit connection and PWM control, are addressed based on hybrid energy pumping. Moreover, for any one of these converters, the power switches are easy to drive via one half-bridge gate driver and one low-side gate driver. From the experimental results, such converters display good steady-state and transient-state performances, and hence are suitable for industrial applications. In addition, the voltage stress on the low-side switch to magnetise the inductor and the voltage stress on the output diode can be reduced as compared to the traditional boost converter.

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